LM393B、LM2903B、LM193、LM293、LM393 和 LM2903 双路比较器

1 特性

- 新增了 LM393B 和 LM2903B
- 改进了 B 版本的规格
  - 最大额定值：高达 38V
  - ESD 等级 (HBM)：2kV
  - 低输入失调电压：0.37mV
  - 低输入偏置电流：3.5nA
  - 低电源电流：每个比较器 200µA
  - 更短的响应时间（1 微秒）
  - LM393B 的工作温度范围
  - 采用 2 x 2mm 微型 WSON 封装
- B 版本可直接取代 LM293、LM393 和 LM2903 的 A 和 V 版本
- 共模输入电压范围包括接地
- 差分输入电压范围等于最大额定电源电压：±38V
- 低输出饱和电压
- 输出与 TTL、MOS 和 CMOS 兼容

2 应用

- 扫地机器人
- 单相 UPS
- 服务器 PSU
- 无线电动工具
- 无线基础设施
- 电器
- 楼宇自动化
- 工厂自动化与控制
- 电机驱动器
- 信息娱乐系统与仪表组

3 说明

LM393B 和 LM2903B 器件是业界通用 LM393 和 LM2903 比较器系列的下一代版本。下一代 B 版本比较器为成本敏感型应用提供了卓越的价值，具有更低的失调电压、更高的电源电压能力、更低的电源电流、更低的输入偏置电流和更低的传播延迟，并通过专用 ESD 钳位提高了 2kV ESD 性能和输入耐用性。LM393B 和 LM2903B 可直接替代 LM293、LM393 和 LM2903（“A”和“V”版本）。

所有器件都包含两个独立的电压比较器，这些比较器可在宽电压范围内由单电源供电运行。静态电流与电源电压无关，输出可连接至其他集电极开路输出，以实现线与逻辑。

器件信息

器件型号	封装[(1)]	封装尺寸（标称值）
LM393B、LM2903B、LM193、LM293、LM293A、LM393、LM393A、LM2903、LM2903V、LM2903AV	SOIC (8)	4.90mm x 3.91mm
LM393B、LM2903B、LM293、LM293A、LM393、LM393A、LM2903	VSSOP (8)	3.00mm x 3.00mm
LM293、LM393、LM393A、LM2903	PDIP (8)	9.81mm × 6.35mm
LM393、LM393A、LM2903	SO (8)	6.20mm x 5.30mm
LM393B、LM2903B、LM393、LM393A、LM2903、LM2903V、LM2903AV	TSSOP (8)	3.00mm x 4.40mm
LM393B	SOT-23 (8)	2.90mm x 1.60mm
LM393B、LM2903B	WSON (8)	2.00mm × 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision AC (February 2020) to Revision AD (October 2020) — **Page**

- 更新了整个文档的表、图和交叉参考的编号格式。 1

Changes from Revision AB (December 2019) to Revision AC (February 2020) — **Page**

- 更改了首页的“特性”、“应用”和“说明”文本，以突出 B 版本 1
- 添加了 WSON 和 SOT-23-8 封装 1
- Added Links to Family Table 3
- Added DDF and DSG pkgs to Thermal Table 7

Changes from Revision AA (September 2019) to Revision AB (December 2019) — **Page**

- 将 LM393B 和 LM2903B 的状态从“预发布”更改为“正在供货” 1
- Added Family Comparison Table 3

Changes from Revision Z (October 2017) to Revision AA (September 2019) — **Page**

- 在整个数据表中添加了“B”器件并更改了多处文本 1
- 删除了“器件信息”中旧的 LM193 CDIP 和 LCCC 封装参考和图，这些内容包含在 LM139-MIL 数据表中 1
- Added "B" devices Thermal Information table 7
- Added "B" device electrical tables 7
- Added "B" device graphs 13

5 Family Comparison Table

Specification	LM393B	LM2903B	LM393 LM393A	LM2903	LM2903V LM2903AV	LM193	LM293 LM293A	Units
Supply Votlage	3 to 36	3 to 36	2 to 30	2 to 30	2 to 32	2 to 30	2 to 30	V
Total Supply Current (5V to 36V max)	0.6 to 0.8	0.6 to 0.8	1 to 2.5	1 to 2.5	1 to 2.5	1 to 2.5	1 to 2.5	mA
Temperature Range	−40 to 85	−40 to 125	0 to 70	−40 to 125	−40 to 125	−55 to 125	−25 to 85	°C
ESD (HBM)	2000	2000	1000	1000	1000	1000	1000	V
Offset Voltage (Max over temp)	± 4	± 4	± 9 ± 4	± 15	± 15 ± 4	± 9	± 9 ± 4	V
Input Bias Current (typ / max)	3.5 / 25	3.5 / 25	25 / 250	25 / 250	25 / 250	25 / 100	25 / 250	nA
Response Time (typ)	1	1	1.3	1.3	1.3	1.3	1.3	µsec

6 Pin Configuration and Functions

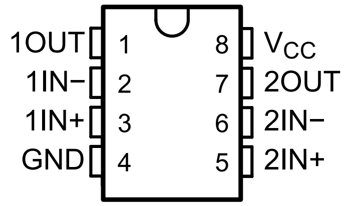
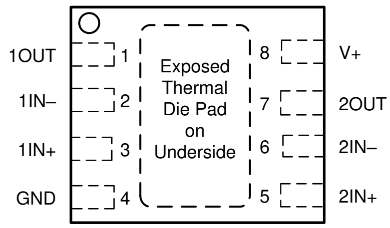


图 6-1. D, DGK, JG, P, PS, DDF or PW Package 8-Pin SOIC, VSSOP, PDIP, SO, or TSSOP Top View



Connect thermal pad directly to GND pin.

图 6-2. DSG Package 8-Pin WSON With Exposed Pad Top View

表 6-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC, VSSOP, PDIP, SO, DDF and TSSOP	DSG		
1OUT	1	1	Output	Output pin of comparator 1
1IN –	2	2	Input	Negative input pin of comparator 1
1IN+	3	3	Input	Positive input pin of comparator 1
GND	4	4	—	Ground
2IN+	5	5	Input	Positive input pin of comparator 2
2IN-	6	6	Input	Negative input pin of comparator 2
2OUT	7	7	Output	Output pin of comparator 2
V_{CC}	8	8	—	Positive Supply
Thermal Pad	—	PAD	—	Connect directly to GND pin

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage[(2)]	Non-B Versions	–0.3	36	V
		B Versions Only		38	
V_{ID}	Differential input voltage[(3)]	Non-B Versions	-36	36	V
		B Versions Only	-38	38	
V_I	Input voltage (either input)	Non-B Versions	–0.3	36	V
		B Versions Only		38	
I_{IK}	Input current[(5)]			-50	mA
V_O	Output voltage	Non-B Versions	–0.3	36	V
		B Versions Only		38	
I_O	Output current	Non-B Versions		20	mA
		B Versions Only		25	
I_{SC}	Duration of output short circuit to ground[(4)]		Unlimited		
T_J	Operating virtual-junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Production Processing Does Not Necessarily Include Testing of All Parameters.
(2) All voltage values, except differential voltages, are with respect to network ground.
(3) Differential voltages are at IN+ with respect to IN–.
(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
(5) Input current flows thorough parasitic diode to ground and turns on parasitic transistors that increases I_{CC} and may cause output to be incorrect. Normal operation resumes when input current is removed.

7.2 ESD Ratings

			VALUE	UNIT
LM393B and LM2903B Only				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1000	
All Other Versions				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	non-V devices	2	30	V
	V devices	2	32	
	"B" version devices	3	36	
Input voltage range, V_{IVR}	non-B devices	0	(V+) – 2.0	V
	"B" version devices	–0.1		
Ambient temperature, T_A	LM193	–55	125	°C
	LM2903, LM2903V, LM2903AV, LM2903B	–40	125	
	LM393B	–40	85	
	LM293, LM293A	–25	85	
	LM393, LM393A	0	70	

7.4 Thermal Information: LM193

THERMAL METRIC(1)		LM193 D (SOIC) 8 pin	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	64.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: LM293, LM393, LM2903 (all 'V' and 'A' suffixes)

THERMAL METRIC(1)		LM293, LM393, LM2903					UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	PS (SO)	PW (TSSOP)	
		8 pin	8 pin	8 pin	8 pin	8 pin	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	131.8	199.4	73.7	139	194.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.4	90.2	62.6	98.9	77.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.2	120.8	50.8	83.7	123.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	26.5	21.5	39.2	47.4	13.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	71.1	119.1	50.7	83	121.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Thermal Information: LM393B and LM2903B

THERMAL METRIC[(1)]		LM393B, LM2903B					UNIT
		D (SOIC)	PW (TSSOP)	DGK (VSSOP)	DDF (SOT-23)	DSG (WSON)	
		8 pin	8 pin	8 pin	8 pin	8 pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	148.5	200.6	193.7	197.9	96.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	90.2	89.6	82.9	119.2	119.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.8	131.3	115.5	115.4	63.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	38.5	22.1	20.8	19.4	12.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	91.1	129.6	113.9	113.7	63.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	-	-	37.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.7 Electrical Characteristics LM393B

V_S = 5 V, V_{CM} = (V –) ; T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_S = 5 to 36V	–2.5	±0.37	2.5	mV
		V_S = 5 to 36V, T_A = –40°C to +85°C	–4		4	
I_B	Input bias current			–3.5	–25	nA
		T_A = –40°C to +85°C			–50	nA
I_{OS}	Input offset current		–10	±0.5	10	nA
		T_A = –40°C to +85°C	–25		25	nA
V_{CM}	Common mode range	V_S = 3 to 36V	(V –)		(V+) – 1.5	V
V_{CM}	Common mode range	V_S = 3 to 36V, T_A = –40°C to +85°C	(V –)		(V+) – 2.0	V
A_{VD}	Large signal differential voltage amplification	V_S = 15V, V_O = 1.4V to 11.4V; $R_L \geq$ 15k to (V+)	50	200		V/mV
V_{OL}	Low level output Voltage {swing from (V –)}	$I_{SINK} \leq$ 4mA, V_{ID} = -1V		110	400	mV
		$I_{SINK} \leq$ 4mA, V_{ID} = -1V T_A = –40°C to +85°C			550	mV
I_{OH-LKG}	High-level output leakage current	(V+) = V_O = 5 V; V_{ID} = 1V		0.1	20	nA
		(V+) = V_O = 36V; V_{ID} = 1V		0.3	50	nA
I_{OL}	Low level output current	V_{OL} = 1.5V; V_{ID} = -1V; V_S = 5V	6	21		mA
I_Q	Quiescent current (all comparators)	V_S = 5 V, no load		400	600	µA
		V_S = 36 V, no load, T_A = –40°C to +85°C		550	800	µA

7.8 Electrical Characteristics LM2903B

V_S = 5 V, V_{CM} = (V –) ; T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_S = 5 to 36V	– 2.5	±0.37	2.5	mV
		V_S = 5 to 36V, T_A = – 40°C to +125°C	– 4		4	
I_B	Input bias current			– 3.5	– 25	nA
		T_A = – 40°C to +125°C			– 50	nA
I_{OS}	Input offset current		– 10	±0.5	10	nA
		T_A = – 40°C to +125°C	– 25		25	nA
V_{CM}	Common mode range	V_S = 3 to 36V	(V –)		(V+) – 1.5	V
		V_S = 3 to 36V, T_A = – 40°C to +125°C	(V –)		(V+) – 2.0	V
A_{VD}	Large signal differential voltage amplification	V_S = 15V, V_O = 1.4V to 11.4V; $R_L \geqslant$ 15k to (V+)	50	200		V/mV
V_{OL}	Low level output Voltage {swing from (V –)}	$I_{SINK} \leqslant$ 4mA, V_{ID} = -1V		110	400	mV
		$I_{SINK} \leqslant$ 4mA, V_{ID} = -1V T_A = – 40°C to +125°C			550	mV
I_{OH-LKG}	High-level output leakage current	(V+) = V_O = 5 V; V_{ID} = 1V		0.1	20	nA
		(V+) = V_O = 36V; V_{ID} = 1V		0.3	50	nA
I_{OL}	Low level output current	V_{OL} = 1.5V; V_{ID} = -1V; V_S = 5V	6	21		mA
I_Q	Quiescent current (all comparators)	V_S = 5 V, no load		400	600	µA
		V_S = 36 V, no load, T_A = – 40°C to +125°C		550	800	µA

7.9 Switching Characteristics LM393B and LM2903B

V_S = 5V, V_{O_PULLUP} = 5V, V_{CM} = V_S/2, C_L = 15pF, R_L = 5.1k Ohm, T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{response}$	Propagation delay time, high-to-low; TTL input signal (1)	TTL input with V_{ref} = 1.4V		300		ns
$t_{response}$	Propagation delay time, high-to-low; Small scale input signal (1)	Input overdrive = 5mV, Input step = 100mV		1000		ns

(1) High-to-low and low-to-high refers to the transition at the input.

7.10 Electrical Characteristics for LM193, LM293, and LM393 (without A suffix)

at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	LM193			LM293 LM393			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_{IC} = V_{ICR} min, V_O = 1.4 V		25°C		2	5		2	5	mV
				Full range			9			9	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		3	25		5	50	nA
				Full range			100			250	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		–25	–100		–25	–250	nA
				Full range			–300			–400	
V_{ICR}	Common-mode input-voltage range(2)			25°C	0 to V_{CC} – 1.5			0 to V_{CC} – 1.5			V
				Full range	0 to V_{CC} – 2			0 to V_{CC} – 2			
A_{VD}	Large-signal differential-voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, R_L ≥ 15 kΩ to V_{CC}		25°C	50	200		50	200		V/mV
I_{OH}	High-level output current	V_{OH} = 5 V	V_{ID} = 1 V	25°C		0.1			0.1	50	nA
		V_{OH} = 30 V	V_{ID} = 1 V	Full range			1			1	μA
V_{OL}	Low-level output voltage	I_{OL} = 4 mA,	V_{ID} = –1 V	25°C		150	400		130	400	mV
				Full range			700			700	
I_{OL}	Low-level output current	V_{OL} = 1.5 V,	V_{ID} = –1 V	25°C	6			6			mA
I_{CC}	Supply current	R_L = ∞	V_{CC} = 5 V	25°C		0.8	1		0.45	1	mA
			V_{CC} = 30 V	Full range			2.5		0.55	2.5	

(1) Full range (minimum or maximum) for LM193 is –55°C to 125°C, for LM293 is –25°C to 85°C, and for LM393 is 0°C to 70°C. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.

(2) The voltage at either input should not be allowed to go negative by more than 0.3 V otherwise output may be incorrect and excessive input current can flow. The upper end of the common-mode voltage range is limited by V_{CC} – 2V. However only one input needs to be in the valid common mode range, the other input can go up the maximum V_{CC} level and the comparator provides a proper output state. Either or both inputs can go to maximum V_{CC} level without damage.

7.11 Electrical Characteristics for LM293A and LM393A

at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	LM293A LM393A MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_O = 1.4 V $V_{IC} = V_{ICR(min)}$		25°C		1	2	mV
				Full range			4	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		5	50	nA
				Full range			150	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		–25	–250	nA
				Full range			–400	
V_{ICR}	Common-mode input-voltage range(2)			25°C	0 to V_{CC} – 1.5			V
				Full range	0 to V_{CC} – 2			
A_{VD}	Large-signal differential-voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, $R_L \geqslant$ 15 kΩ to V_{CC}		25°C	50	200		V/mV
I_{OH}	High-level output current	V_{OH} = 5 V,	V_{ID} = 1 V	25°C		0.1	50	nA
		V_{OH} = 30 V,	V_{ID} = 1 V	Full range			1	μA
V_{OL}	Low-level output voltage	I_{OL} = 4 mA,	V_{ID} = –1 V	25°C		110	400	mV
				Full range			700	
I_{OL}	Low-level output current	V_{OL} = 1.5 V,	V_{ID} = –1 V,	25°C	6			mA
I_{CC}	Supply current	$R_L = \infty$	V_{CC} = 5 V	25°C		0.60	1	mA
			V_{CC} = 30 V	Full range		0.72	2.5	

(1) Full range (minimum or maximum) for LM293A is –25°C to 85°C, and for LM393A is 0°C to 70°C. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.

(2) The voltage at either input should not be allowed to go negative by more than 0.3 V otherwise output may be incorrect and excessive input current can flow. The upper end of the common-mode voltage range is limited by V_{CC} – 2V. However only one input needs to be in the valid common mode range, the other input can go up the maximum V_{CC} level and the comparator provides a proper output state. Either or both inputs can go to maximum V_{CC} level without damage.

7.12 Electrical Characteristics for LM2903, LM2903V, and LM2903AV

at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	LM2903, LM2903V			LM2903AV			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to MAX(2), V_O = 1.4 V, V_{IC} = $V_{ICR(min)}$,		25°C		2	7		1	2	mV
				Full range			15			4	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		5	50		5	50	nA
				Full range			200			200	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		–25	–250		–25	–250	nA
				Full range			–500			–500	
V_{ICR}	Common-mode input-voltage range(3)			25°C	0 to V_{CC} – 1.5			0 to V_{CC} – 1.5			V
				Full range	0 to V_{CC} – 2			0 to V_{CC} – 2			
A_{VD}	Large-signal differential-voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, $R_L \geq$ 15 kΩ to V_{CC}		25°C	25	100		25	100		V/mV
I_{OH}	High-level output current	V_{OH} = 5 V,	V_{ID} = 1 V	25°C		0.1	50		0.1	50	nA
		V_{OH} = V_{CC} MAX(2),	V_{ID} = 1 V	Full range			1			1	μA
V_{OL}	Low-level output voltage	I_{OL} = 4 mA,	V_{ID} = –1 V,	25°C		150	400		150	400	mV
				Full range			700			700	
I_{OL}	Low-level output current	V_{OL} = 1.5 V,	V_{ID} = –1 V	25°C	6			6			mA
I_{CC}	Supply current	R_L = ∞	V_{CC} = 5 V	25°C		0.8	1		0.8	1	mA
			V_{CC} = MAX	Full range			2.5			2.5	

(1) Full range (minimum or maximum) for LM2903 is –40°C to 125°C. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
(2) V_{CC} MAX = 30 V for non-V devices and 32 V for V-suffix devices.
(3) The voltage at either input should not be allowed to go negative by more than 0.3 V otherwise output may be incorrect and excessive input current can flow. The upper end of the common-mode voltage range is limited by V_{CC} – 2V. However only one input needs to be in the valid common mode range, the other input can go up the maximum V_{CC} level and the comparator provides a proper output state. Either or both inputs can go to maximum V_{CC} level without damage.

7.13 Switching Characteristics: LM193, LM239, LM393, LM2903, all 'A' and 'V' versions

V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TYP	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF(1) (2)	100-mV input step with 5-mV overdrive	1.3	μs
		TTL-level input step	0.3	

(1) C_L includes probe and jig capacitance.
(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

7.14 Typical Characteristics, LMx93, LM2903 (all 'V' and 'A' suffixes)

T_A= 25°C, V_S= 5V, R_{PULLUP}=5.1k, C_L = 15 pF, V_{CM}=0V unless otherwise noted.

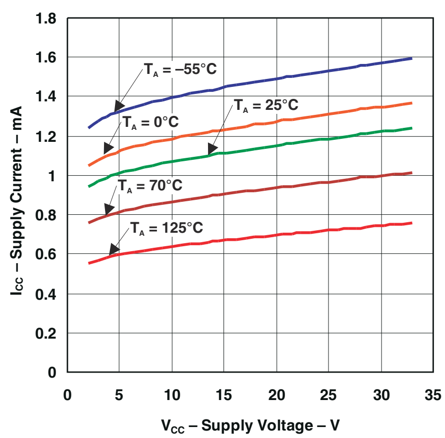


图 7-1. Supply Current vs Supply Voltage

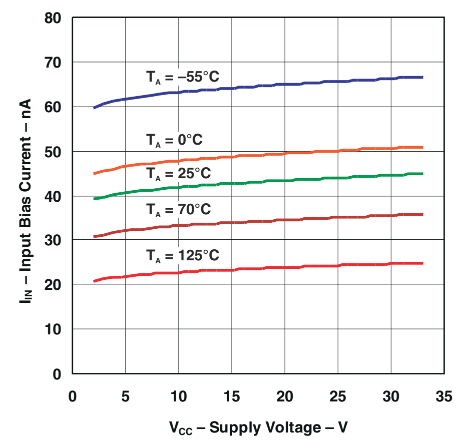


图 7-2. Input Bias Current vs Supply Voltage

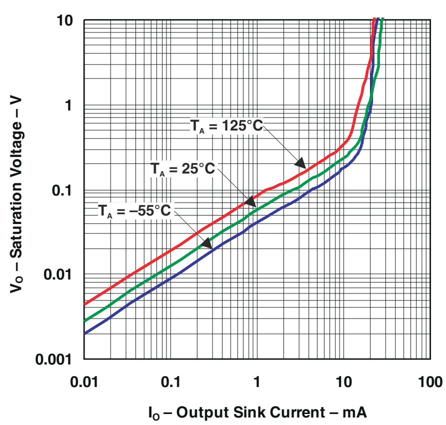


图 7-3. Output Saturation Voltage

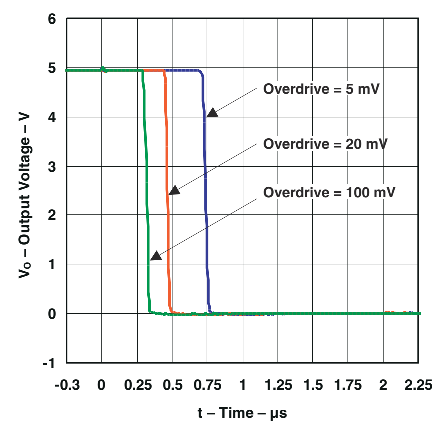


图 7-4. Response Time for Various Overdrives Negative Transition

7.14 Typical Characteristics, LMx93, LM2903 (all 'V' and 'A' suffixes) (continued)

T_A= 25°C, V_S= 5V, R_{PULLUP}=5.1k, C_L = 15 pF, V_{CM}=0V unless otherwise noted.

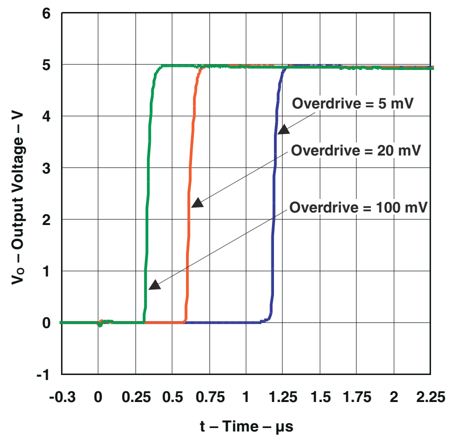


图 7-5. Response Time for Various Overdrives Positive Transition

7.15 Typical Characteristics, LM393B and LM2903B

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

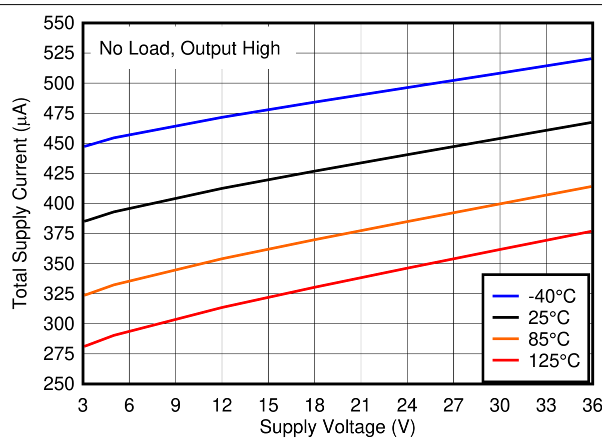


图 7-6. Total Supply Current vs. Supply Voltage

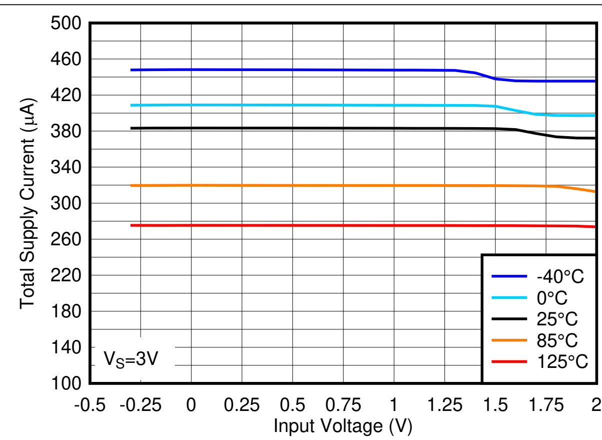


图 7-7. Total Supply Current vs. Input Voltage at 3V

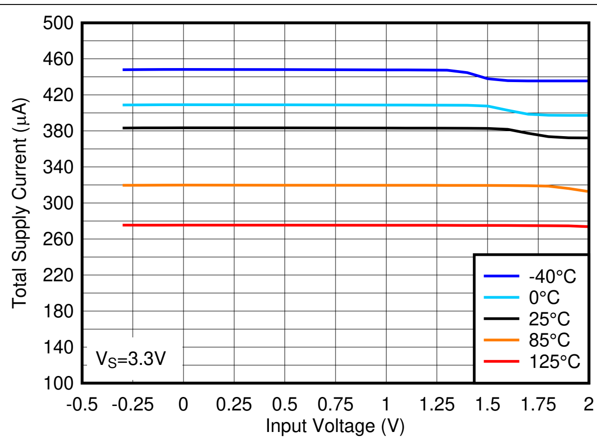


图 7-8. Total Supply Current vs. Input Voltage at 3.3V

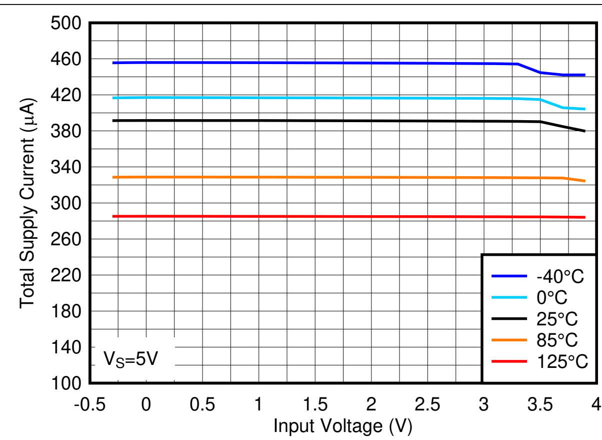


图 7-9. Total Supply Current vs. Input Voltage at 5V

7.15 Typical Characteristics, LM393B and LM2903B (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

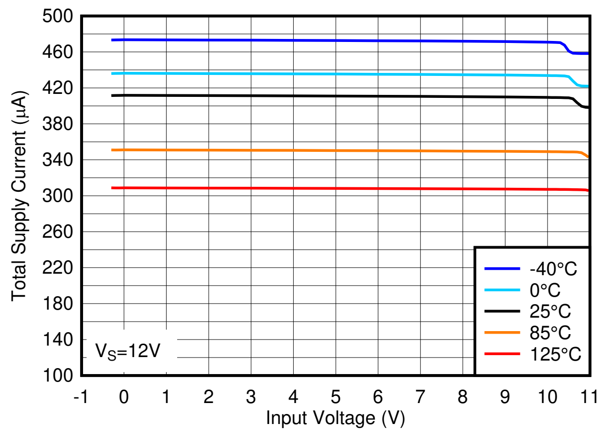


图 7-10. Total Supply Current vs. Input Voltage at 12V

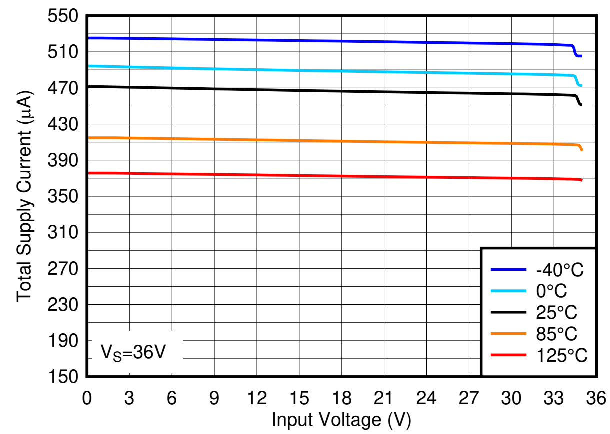


图 7-11. Total Supply Current vs. Input Voltage at 36V

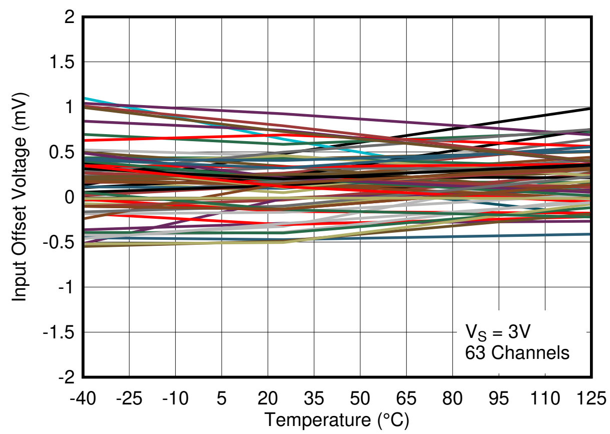


图 7-12. Input Offset Voltage vs. Temperature at 3V

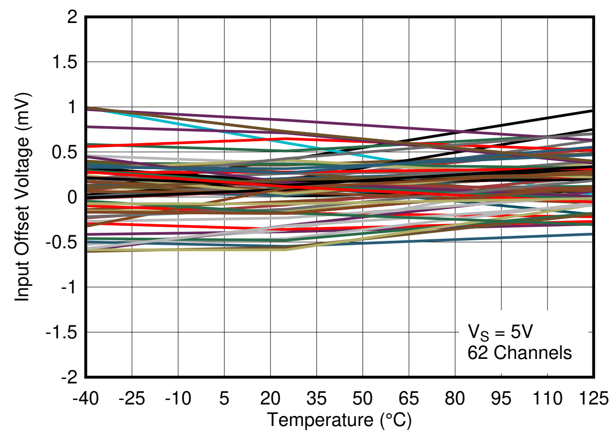


图 7-13. Input Offset Voltage vs. Temperature at 5V

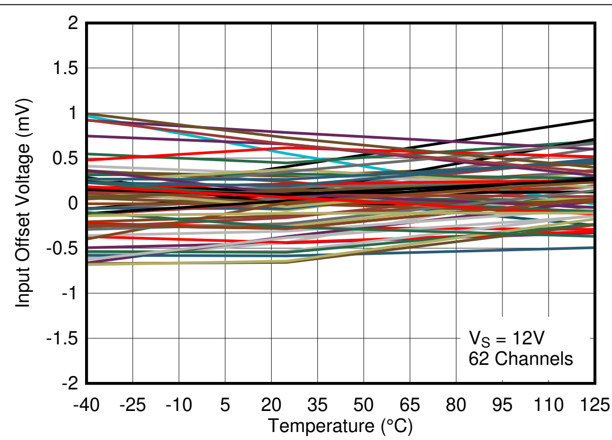


图 7-14. Input Offset Voltage vs. Temperature at 12V

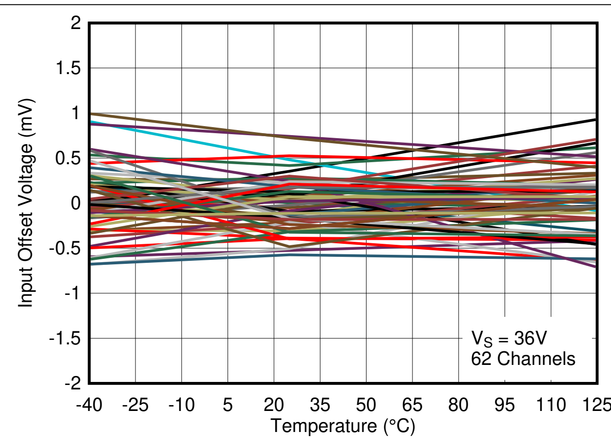


图 7-15. Input Offset Voltage vs. Temperature at 36

7.15 Typical Characteristics, LM393B and LM2903B (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

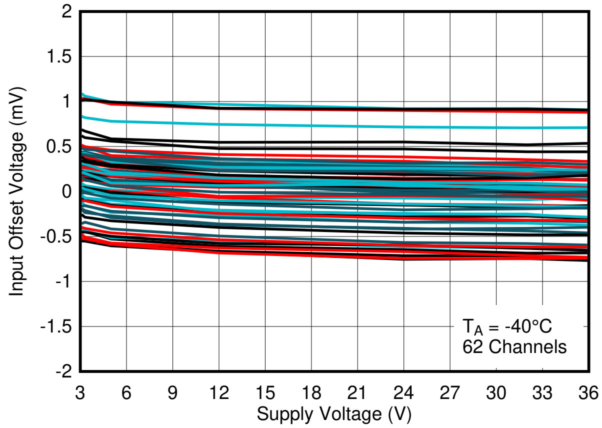


图 7-16. Input Offset Voltage vs. Supply Voltage at -40°C

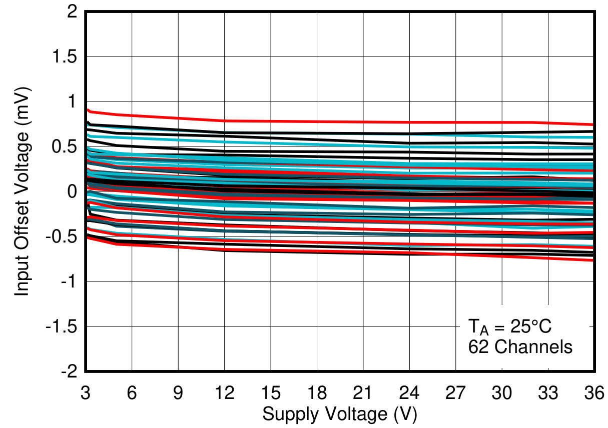


图 7-17. Input Offset Voltage vs. Supply Voltage at 25°C

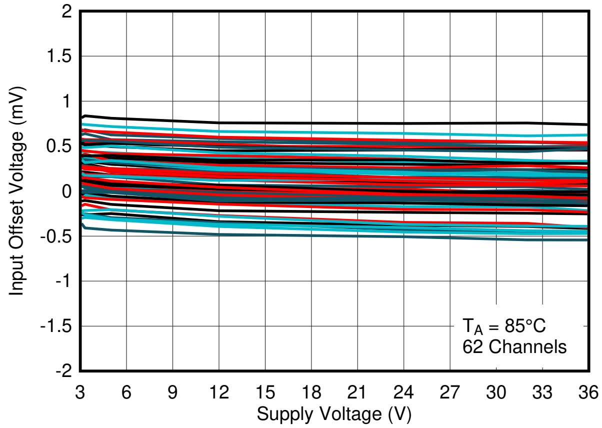


图 7-18. Input Offset Voltage vs. Supply Voltage at 85°C

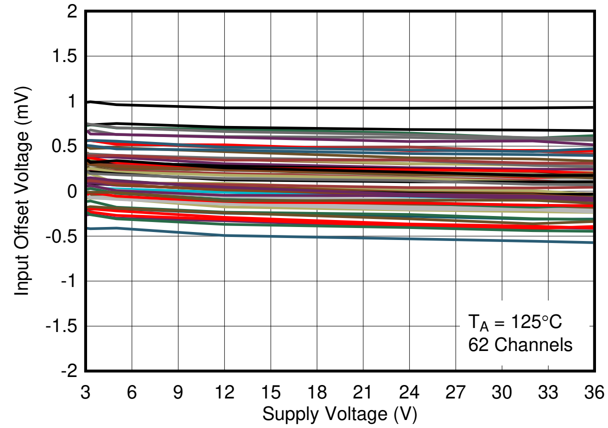


图 7-19. Input Offset Voltage vs. Supply Voltage at 125°C

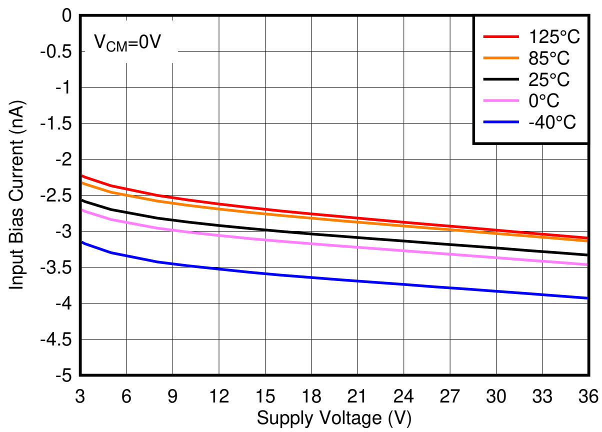


图 7-20. Input Bias Current vs. Supply Voltage

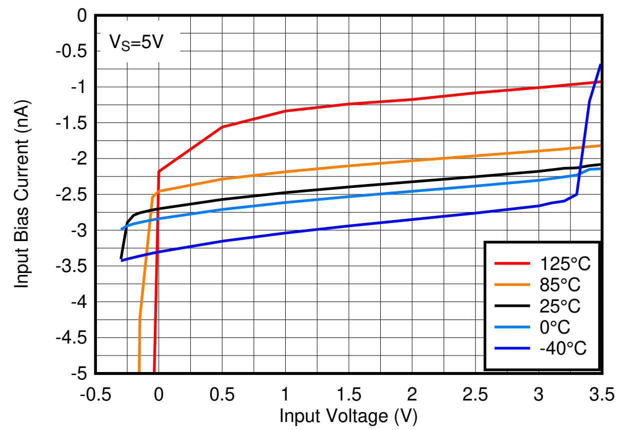


图 7-21. Input Bias Current vs. Input Voltage at 5V

7.15 Typical Characteristics, LM393B and LM2903B (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

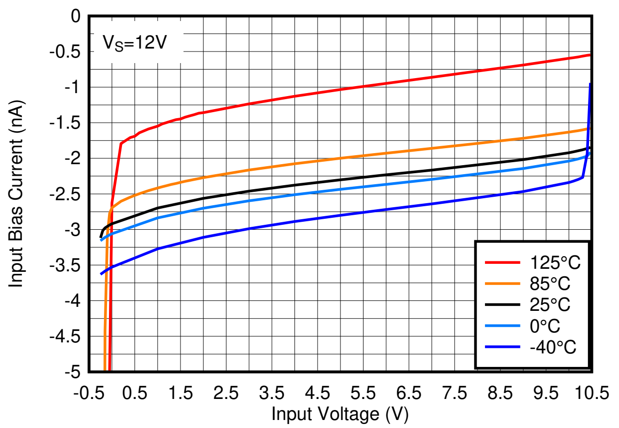


图 7-22. Input Bias Current vs. Input Voltage at 12V

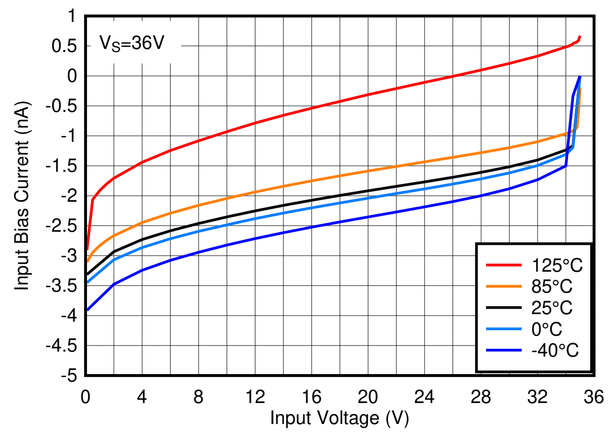


图 7-23. Input Bias Current vs. Input Voltage at 36V

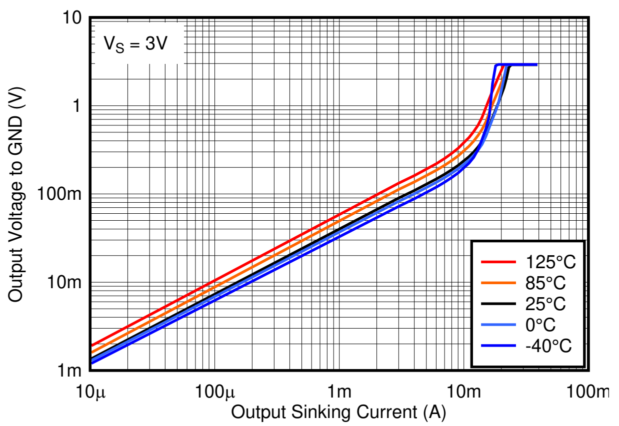


图 7-24. Output Low Voltage vs. Output Sinking Current at 3V

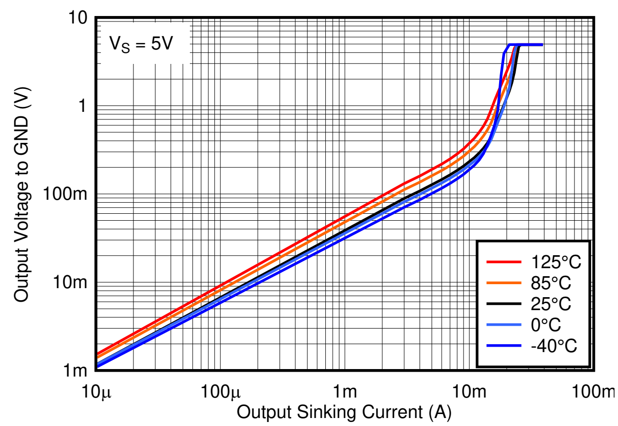


图 7-25. Output Low Voltage vs. Output Sinking Current at 5V

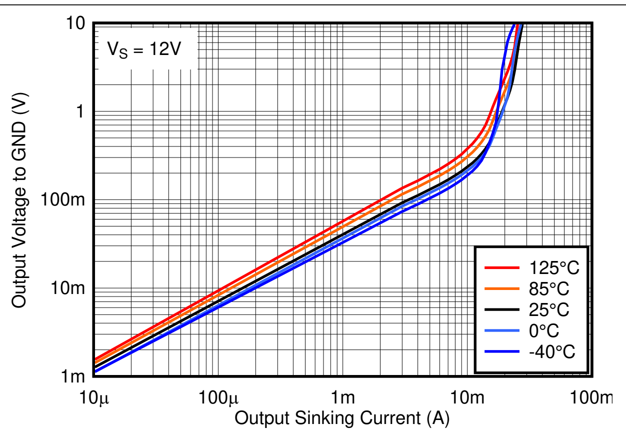


图 7-26. Output Low Voltage vs. Output Sinking Current at 12V

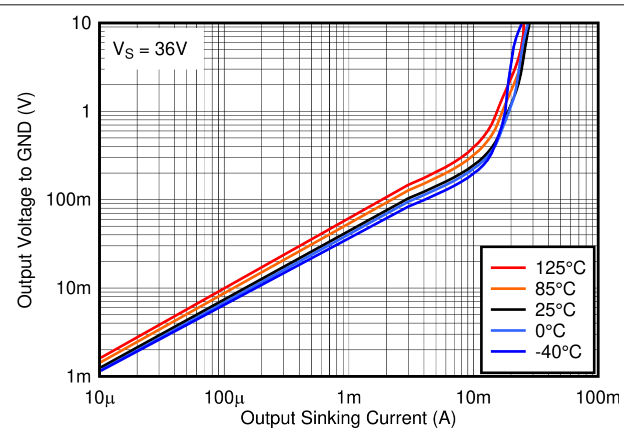


图 7-27. Output Low Voltage vs.Output Sinking Current at 36V

7.15 Typical Characteristics, LM393B and LM2903B (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

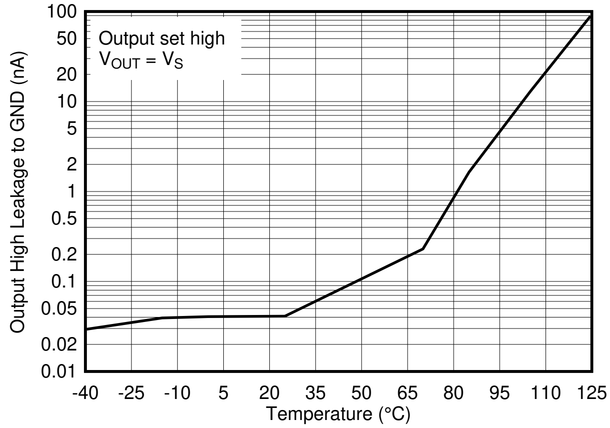


图 7-28. Output High Leakage Current vs.Temperature at 5V

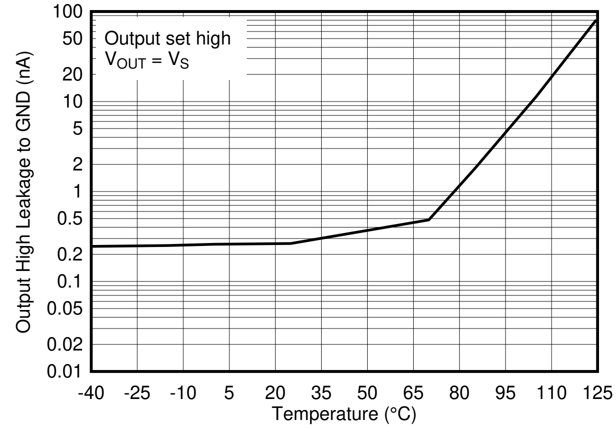


图 7-29. Output High Leakage Current vs. Temperature at 36V

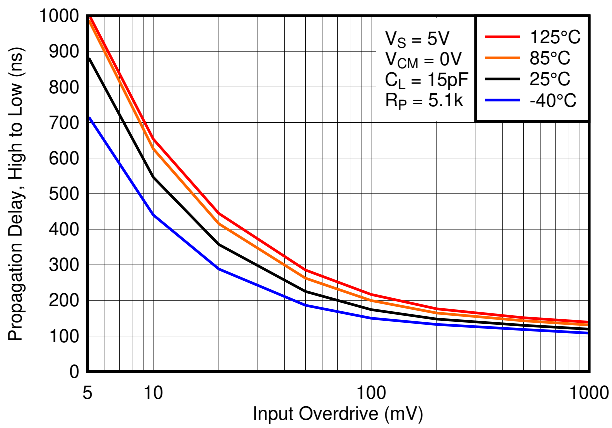


图 7-30. High to Low Propagation Delay vs. Input Overdrive Voltage, 5V

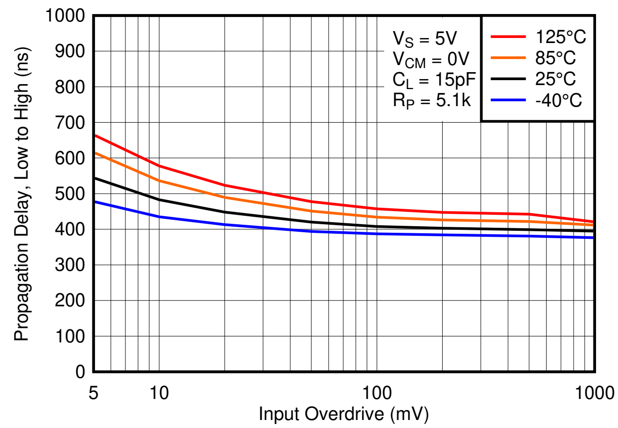


图 7-31. Low to High Propagation Delay vs. Input Overdrive Voltage, 5V

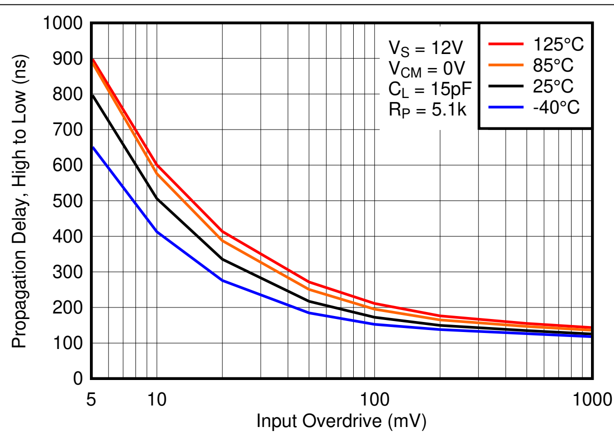


图 7-32. High to Low Propagation Delay vs. Input Overdrive Voltage, 12V

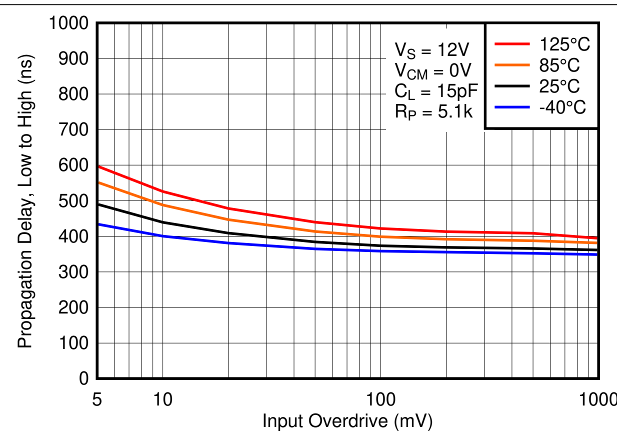


图 7-33. Low to High Propagation Delay vs. Input Overdrive Voltage, 12V

7.15 Typical Characteristics, LM393B and LM2903B (continued)

T_A = 25°C, V_S = 5 V, R_{PULLUP} = 5.1k, C_L = 15 pF, V_{CM} = 0 V, $V_{UNDERDRIVE}$ = 100 mV, $V_{OVERDRIVE}$ = 100 mV unless otherwise noted.

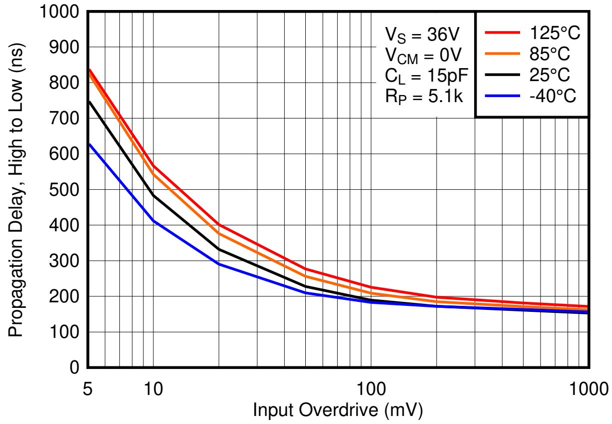


图 7-34. High to Low Propagation Delay vs. Input Overdrive Voltage, 36V

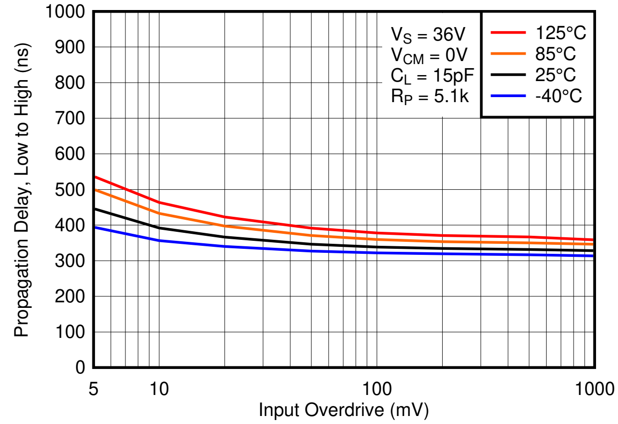


图 7-35. Low to High Propagation Delay vs. Input Overdrive Voltage, 36V

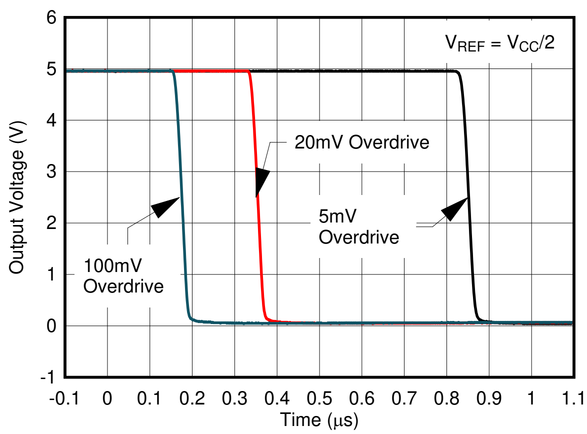


图 7-36. Response Time for Various Overdrives, High-to-Low Transition

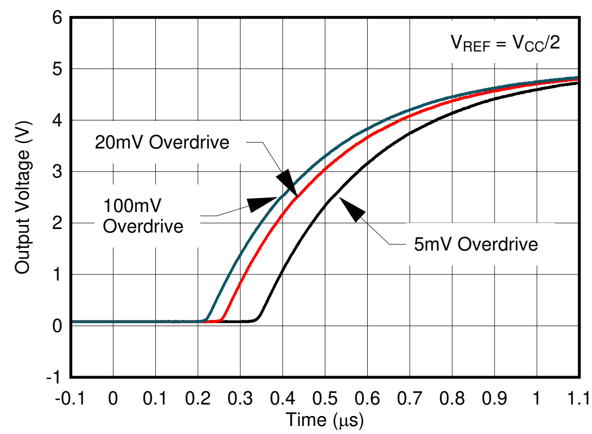


图 7-37. Response Time for Various Overdrives, Low-to-High Transition

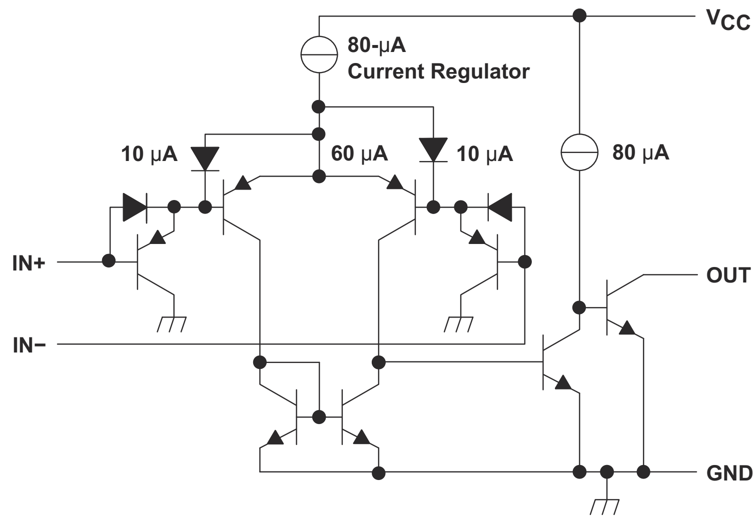
8 Detailed Description

8.1 Overview

These dual comparators have the ability to operate up to absolute maximum of 36 V (38 V for the "B" version) on the supply pin. This device has proven ubiquity and versatility across a wide range of applications. This is due to very wide supply voltages range, low Iq and fast response of the devices.

The open-drain output allows the user to configure the output's logic high voltage (V_{OH}) and can be used to enable the comparator to be used in AND functionality.

8.2 Functional Block Diagram



COMPONENT COUNT	
Epi-FET	1
Diodes	2
Resistors	2
Transistors	30

图 8-1. Schematic (Each Comparator)

8.3 Feature Description

The comparator consists of a PNP darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common mode voltage capability, allowing the comparator to accurately function from ground to V_{CC} – 1.5 V input. Allow for V_{CC} – 2 V at cold temperature.

The output consists of an open drain NPN (pull-down or low side) transistor. The output NPN sinks current when the negative input voltage is higher than the positive input voltage and the offset voltage. The V_{OL} is resistive and scales with the output current. See 图 7-3 for V_{OL} values with respect to the output current.

8.4 Device Functional Modes

8.4.1 Voltage Comparison

The device operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pullup) based on the input differential polarity.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The device is typically used to compare a single signal to a reference or two signals against each other. Many users take advantage of the open drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes this comaprator optimal for level shifting to a higher or lower voltage.

9.2 Typical Application

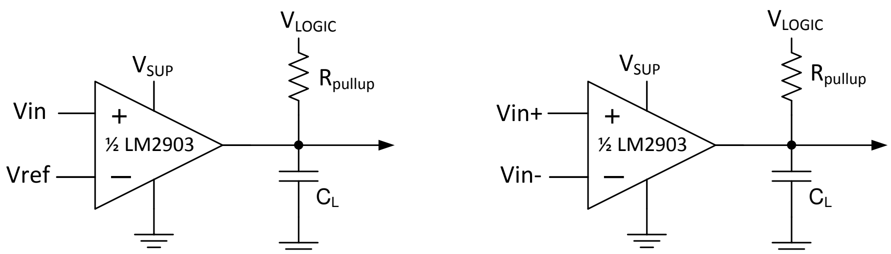


图 9-1. Single-Ended and Differential Comparator Configurations

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 9-1 as the input parameters.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0 V to Vsup-2 V
Supply Voltage	4.5 V to V_{CC} maximum
Logic Supply Voltage	0 V to V_{CC} maximum
Output Current (R_{PULLUP})	1 µA to 4 mA
Input Overdrive Voltage	100 mV
Reference Voltage	2.5 V
Load Capacitance (C_L)	15 pF

9.2.2 Detailed Design Procedure

When using the device in a general comparator application, determine the following:

- Input Voltage Range
- Minimum Overdrive Voltage
- Output and Drive Current
- Response Time

9.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{ICR}) must be taken in to account. If temperature operation is below 25°C the V_{ICR} can range from 0 V to V_{CC} – 2.0 V. This limits the input voltage range to as high as V_{CC} – 2.0 V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

The following is a list of input voltage situation and their outcomes:

1. When both IN- and IN+ are both within the common-mode range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
   b. If IN- is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
2. When IN- is higher than common-mode and IN+ is within common-mode, the output is low and the output transistor is sinking current
3. When IN+ is higher than common-mode and IN- is within common-mode, the output is high impedance and the output transistor is not conducting
4. When IN- and IN+ are both higher than common-mode, the output is low and the output transistor is sinking current

9.2.2.2 Minimum Overdrive Voltage

Overdrive Voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). To make an accurate comparison the Overdrive Voltage (V_{OD}) should be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. 图 9-2 and 图 9-3 show positive and negative response times with respect to overdrive voltage.

9.2.2.3 Output and Drive Current

Output current is determined by the load/pull-up resistance and logic/pullup voltage. The output current produces a output low voltage (V_{OL}) from the comparator. In which V_{OL} is proportional to the output current. Use 节 7.14 to determine V_{OL} based on the output current.

The output current can also effect the transient response. See 节 9.2.2.4 for more information.

9.2.2.4 Response Time

Response time is a function of input over drive. See 节 9.2.3 for typical response times. The rise and falls times can be determined by the load capacitance (C_L), load/pullup resistance (R_{PULLUP}) and equivalent collector-emitter resistance (R_{CE}).

- The rise time (τ_R) is approximately $\tau_R \sim R_{PULLUP} \times C_L$
- The fall time (τ_F) is approximately $\tau_F \sim R_{CE} \times C_L$
  - R_{CE} can be determine by taking the slope of 节 7.14 in its linear region at the desired temperature, or by dividing the V_{OL} by I_{out}

9.2.3 Application Curves

The following curves were generated with 5 V on V_{CC} and V_{Logic}, R_{PULLUP} = 5.1 kΩ, and 50 pF scope probe.

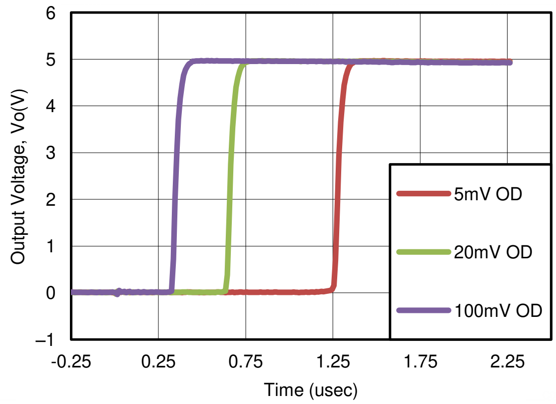


图 9-2. Response Time for Various Overdrives (Positive Transition)

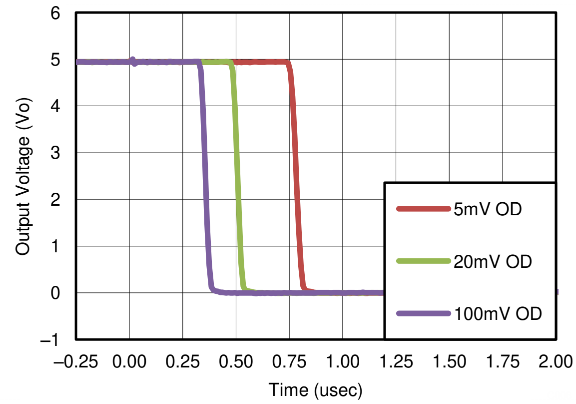


图 9-3. Response Time for Various Overdrives (Negative Transition)

10 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, TI recommends to use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can eat into the input common-mode range of the comparator and create an inaccurate comparison.

11 Layout

11.1 Layout Guidelines

For accurate comparator applications without hysteresis it is important maintain a stable power supply with minimized noise and glitches. To achieve this, it is best to add a bypass capacitor between the supply voltage and ground. This should be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the IC's GND pin and system ground.

Minimize coupling between outputs and inverting inputs to prevent output oscillations. Do not run output and inverting input traces in parallel unless there is a V_{CC} or GND trace between output and inverting input traces to reduce coupling. When series resistance is added to inputs, place resistor close to the device.

11.2 Layout Example

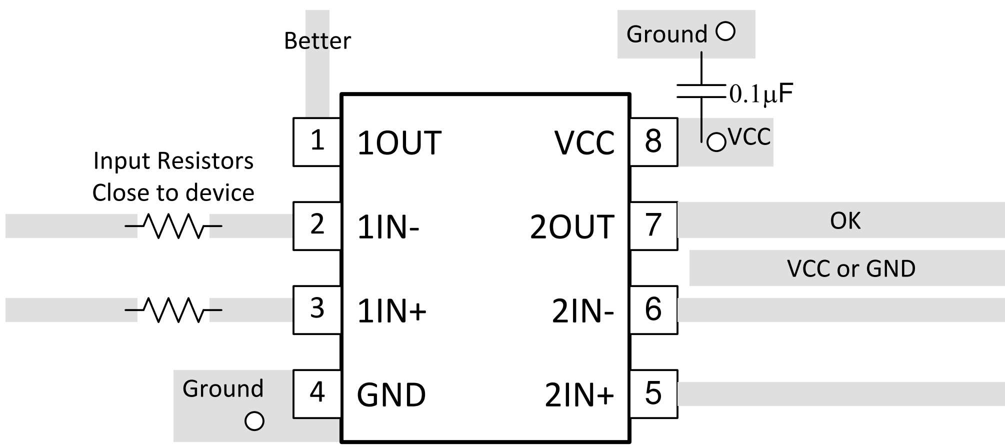


图 11-1. LM2903 Layout Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM193	Click here	Click here	Click here	Click here	Click here
LM293	Click here	Click here	Click here	Click here	Click here
LM293A	Click here	Click here	Click here	Click here	Click here
LM393	Click here	Click here	Click here	Click here	Click here
LM393A	Click here	Click here	Click here	Click here	Click here
LM2903	Click here	Click here	Click here	Click here	Click here
LM2903V	Click here	Click here	Click here	Click here	Click here
LM393B	Click here	Click here	Click here	Click here	Click here
LM2903B	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM193DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM193	Samples
LM193DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM193	Samples
LM2903AVQDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903AV	Samples
LM2903AVQDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903AV	Samples
LM2903AVQPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903AV	Samples
LM2903AVQPWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903AV	Samples
LM2903BIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903B	Samples
LM2903BIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	903B	Samples
LM2903BIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903B	Samples
LM2903BIDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	903B	Samples
LM2903BIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903B	Samples
LM2903D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples
LM2903DE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples
LM2903DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples
LM2903DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(MAP, MAS, MAU)	Samples
LM2903DGKRG4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	(MAP, MAS, MAU)	Samples
LM2903DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples
LM2903DRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples
LM2903DRG3	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples
LM2903DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2903P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	LM2903P	Samples
LM2903PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903	Samples
LM2903PSRG4	ACTIVE	SO	PS	8	2000	TBD	Call TI	Call TI	-40 to 125		Samples
LM2903PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L2903	Samples
LM2903PWRG3	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L2903	Samples
LM2903PWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903	Samples
LM2903QD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q	Samples
LM2903QDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q	Samples
LM2903QDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q	Samples
LM2903VQDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903V	Samples
LM2903VQDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903V	Samples
LM2903VQPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903V	Samples
LM2903VQPWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903V	Samples
LM293AD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293A	Samples
LM293ADE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293A	Samples
LM293ADGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-25 to 85	(MDP, MDS, MDU)	Samples
LM293ADGKRG4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	(MDP, MDS, MDU)	Samples
LM293ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-25 to 85	LM293A	Samples
LM293ADRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293A	Samples
LM293D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293	Samples
LM293DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-25 to 85	(MCP, MCS, MCU)	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM293DGKRG4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-25 to 85	(MCP, MCS, MCU)	Samples
LM293DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-25 to 85	LM293	Samples
LM293DRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293	Samples
LM293DRG3	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-25 to 85	LM293	Samples
LM293DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293	Samples
LM293P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU | SN	N / A for Pkg Type	-25 to 85	LM293P	Samples
LM293PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	LM293P	Samples
LM393AD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393A	Samples
LM393ADE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393A	Samples
LM393ADG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393A	Samples
LM393ADGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(M8P, M8S, M8U)	Samples
LM393ADGKRG4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	(M8P, M8S, M8U)	Samples
LM393ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	LM393A	Samples
LM393ADRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393A	Samples
LM393ADRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393A	Samples
LM393AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU | SN	N / A for Pkg Type	0 to 70	LM393AP	Samples
LM393APE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM393AP	Samples
LM393APSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L393A	Samples
LM393APWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	L393A	Samples
LM393APWRE4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L393A	Samples
LM393APWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L393A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM393BIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	393B	Samples
LM393BIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	393B	Samples
LM393BIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM393B	Samples
LM393BIDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	393B	Samples
LM393BIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM393B	Samples
LM393D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393	Samples
LM393DE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393	Samples
LM393DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393	Samples
LM393DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(M9P, M9S, M9U)	Samples
LM393DGKRG4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	(M9P, M9S, M9U)	Samples
LM393DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	LM393	Samples
LM393DRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393	Samples
LM393DRG3	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	LM393	Samples
LM393DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393	Samples
LM393P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU | SN	N / A for Pkg Type	0 to 70	LM393P	Samples
LM393PE3	ACTIVE	PDIP	P	8	50	RoHS & Non-Green	SN	N / A for Pkg Type	0 to 70	LM393P	Samples
LM393PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM393P	Samples
LM393PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L393	Samples
LM393PSRG4	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L393	Samples
LM393PW	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L393	Samples
LM393PWG4	ACTIVE	TSSOP	PW	8	150	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L393	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM393PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	L393	Samples
LM393PWRG3	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	L393	Samples
LM393PWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L393	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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OTHER QUALIFIED VERSIONS OF LM2903, LM2903B, LM293 :

- Automotive : LM2903-Q1, LM2903B-Q1

- Enhanced Product : LM293-EP

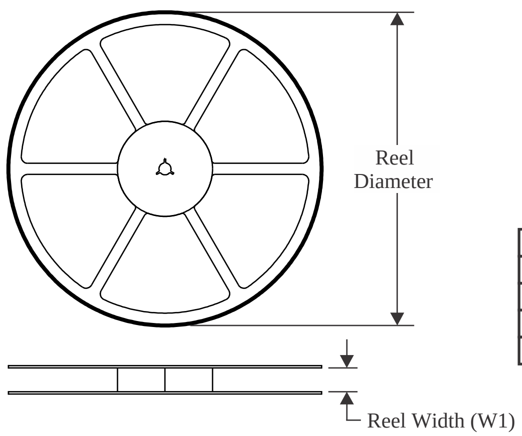
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

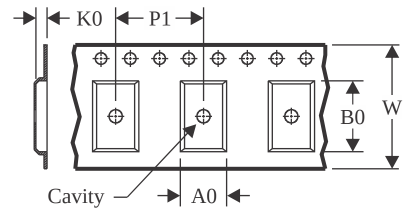
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

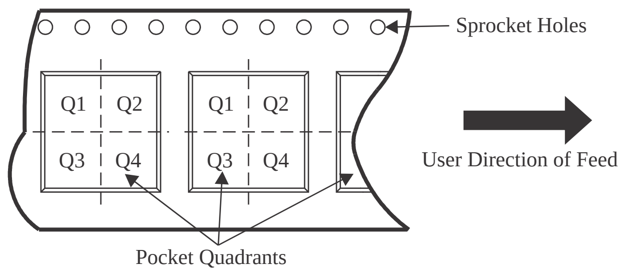


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



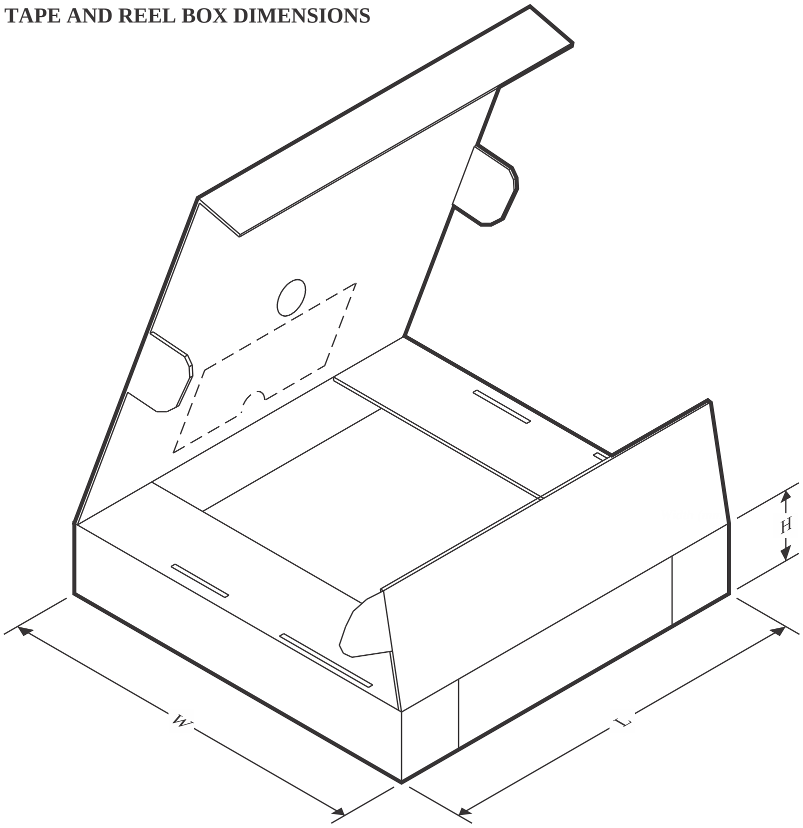
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM193DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903AVQDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2903AVQDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903AVQDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903AVQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903AVQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903BIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2903BIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2903BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903BIDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LM2903BIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2903DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2903DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2903DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM2903DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM2903DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM2903PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903PWRG3	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903QDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903VQDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903VQDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2903VQDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903VQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903VQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903VQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM293ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
LM293ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM293ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM293ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293ADR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM293ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM293DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM293DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM293DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM293DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM293DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
LM393ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM393ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM393ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393APSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM393APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393APWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393BIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM393BIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM393BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393BIDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LM393BIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM393DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM393DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393DRG3	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM393DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM393PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393PWRG3	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



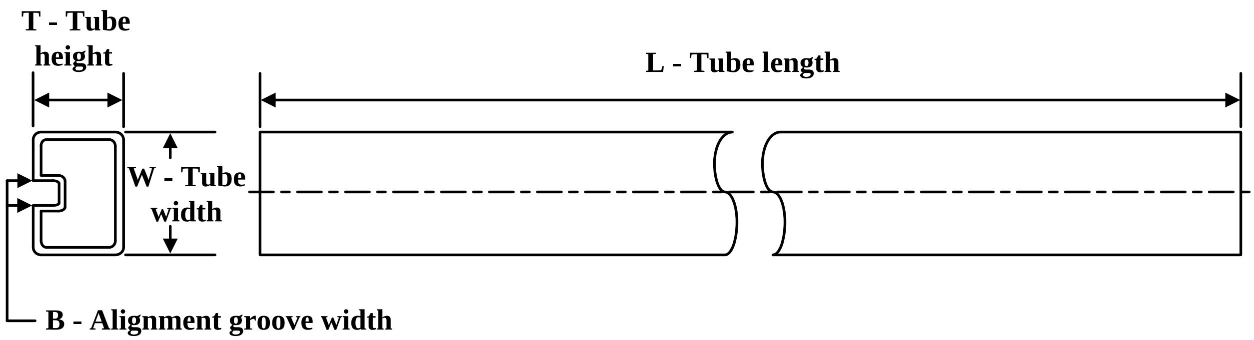
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM193DR	SOIC	D	8	2500	350.0	350.0	43.0
LM2903AVQDR	SOIC	D	8	2500	340.5	336.1	25.0
LM2903AVQDR	SOIC	D	8	2500	340.5	338.1	20.6
LM2903AVQDRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM2903AVQPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2903AVQPWRG4	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2903BIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
LM2903BIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2903BIDR	SOIC	D	8	2500	340.5	336.1	25.0
LM2903BIDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
LM2903BIPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2903DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM2903DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2903DR	SOIC	D	8	2500	356.0	356.0	35.0
LM2903DR	SOIC	D	8	2500	356.0	356.0	35.0
LM2903DR	SOIC	D	8	2500	340.5	338.1	20.6
LM2903DR	SOIC	D	8	2500	364.0	364.0	27.0
LM2903DR	SOIC	D	8	2500	340.5	338.1	20.6

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2903DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM2903DRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM2903DRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM2903DRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM2903DRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM2903PSR	SO	PS	8	2000	356.0	356.0	35.0
LM2903PWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM2903PWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2903PWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2903PWRG3	TSSOP	PW	8	2000	364.0	364.0	27.0
LM2903PWRG4	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2903QDRG4	SOIC	D	8	2500	350.0	350.0	43.0
LM2903VQDR	SOIC	D	8	2500	340.5	338.1	20.6
LM2903VQDR	SOIC	D	8	2500	340.5	338.1	20.6
LM2903VQDRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM2903VQPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2903VQPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2903VQPWRG4	TSSOP	PW	8	2000	356.0	356.0	35.0
LM293ADGKR	VSSOP	DGK	8	2500	370.0	355.0	55.0
LM293ADGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM293ADGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LM293ADR	SOIC	D	8	2500	356.0	356.0	35.0
LM293ADR	SOIC	D	8	2500	340.5	336.1	25.0
LM293ADR	SOIC	D	8	2500	356.0	356.0	35.0
LM293ADR	SOIC	D	8	2500	340.5	338.1	20.6
LM293ADR	SOIC	D	8	2500	364.0	364.0	27.0
LM293ADRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM293ADRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM293ADRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM293ADRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM293DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM293DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM293DR	SOIC	D	8	2500	364.0	364.0	27.0
LM293DR	SOIC	D	8	2500	356.0	356.0	35.0
LM293DR	SOIC	D	8	2500	356.0	356.0	35.0
LM293DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM293DRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM293DRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM293DRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM293DRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM393ADGKR	VSSOP	DGK	8	2500	346.0	346.0	35.0
LM393ADGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM393ADGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM393ADR	SOIC	D	8	2500	340.5	338.1	20.6
LM393ADR	SOIC	D	8	2500	364.0	364.0	27.0
LM393ADR	SOIC	D	8	2500	356.0	356.0	35.0
LM393ADR	SOIC	D	8	2500	356.0	356.0	35.0
LM393ADR	SOIC	D	8	2500	340.5	336.1	25.0
LM393ADRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM393ADRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM393ADRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM393ADRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM393APSR	SO	PS	8	2000	356.0	356.0	35.0
LM393APWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM393APWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM393APWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM393APWRG4	TSSOP	PW	8	2000	356.0	356.0	35.0
LM393BIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
LM393BIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM393BIDR	SOIC	D	8	2500	340.5	336.1	25.0
LM393BIDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
LM393BIPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM393DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM393DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM393DR	SOIC	D	8	2500	356.0	356.0	35.0
LM393DR	SOIC	D	8	2500	356.0	356.0	35.0
LM393DR	SOIC	D	8	2500	340.5	338.1	20.6
LM393DR	SOIC	D	8	2500	340.5	338.1	25.0
LM393DRG3	SOIC	D	8	2500	333.2	345.9	28.6
LM393DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM393DRG4	SOIC	D	8	2500	340.5	336.1	25.0
LM393DRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM393DRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM393DRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM393PSR	SO	PS	8	2000	356.0	356.0	35.0
LM393PWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM393PWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM393PWRG3	TSSOP	PW	8	2000	364.0	364.0	27.0
LM393PWRG4	TSSOP	PW	8	2000	356.0	356.0	35.0

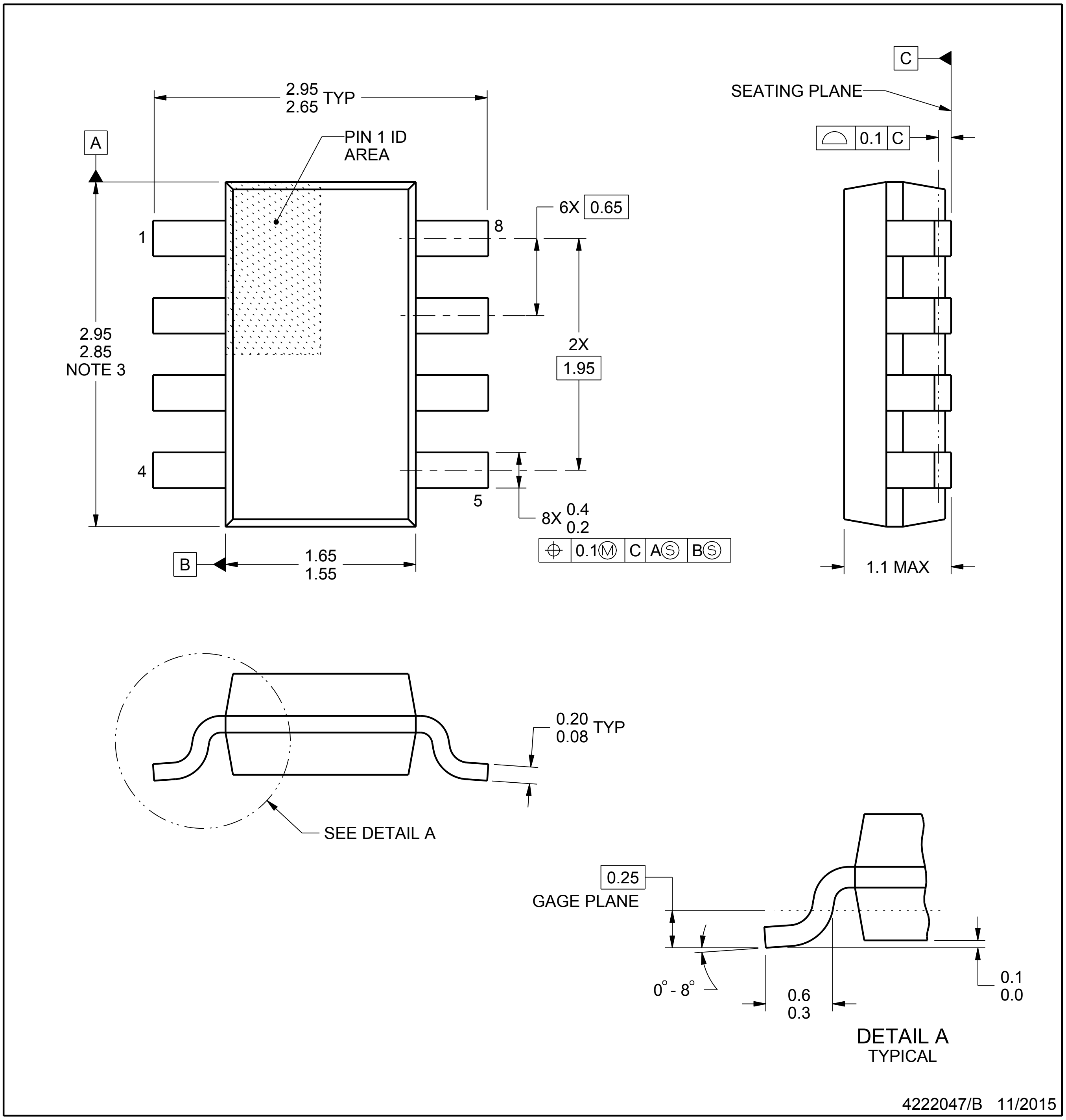
TUBE



*All dimensions are nominal

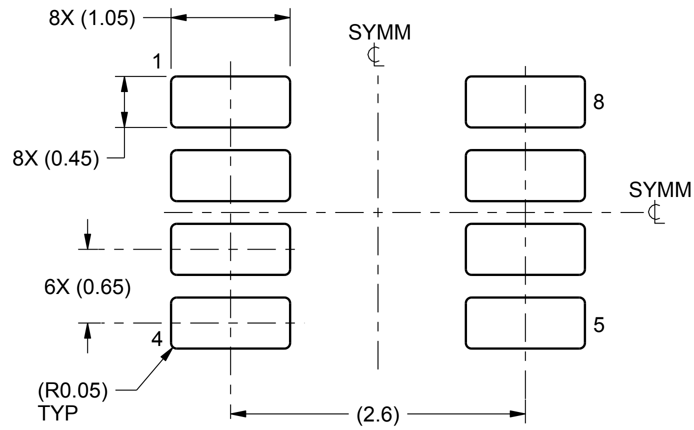
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM2903D	D	SOIC	8	75	506.6	8	3940	4.32
LM2903D	D	SOIC	8	75	507	8	3940	4.32
LM2903DE4	D	SOIC	8	75	506.6	8	3940	4.32
LM2903DE4	D	SOIC	8	75	507	8	3940	4.32
LM2903DG4	D	SOIC	8	75	507	8	3940	4.32
LM2903DG4	D	SOIC	8	75	506.6	8	3940	4.32
LM2903P	P	PDIP	8	50	506	13.97	11230	4.32
LM2903QD	D	SOIC	8	75	505.46	6.76	3810	4
LM2903QDG4	D	SOIC	8	75	505.46	6.76	3810	4
LM293AD	D	SOIC	8	75	507	8	3940	4.32
LM293AD	D	SOIC	8	75	506.6	8	3940	4.32
LM293ADE4	D	SOIC	8	75	507	8	3940	4.32
LM293ADE4	D	SOIC	8	75	506.6	8	3940	4.32
LM293D	D	SOIC	8	75	507	8	3940	4.32
LM293D	D	SOIC	8	75	506.6	8	3940	4.32
LM293P	P	PDIP	8	50	506	13.97	11230	4.32
LM293P	P	PDIP	8	50	506.1	9	600	5.4
LM293PE4	P	PDIP	8	50	506.1	9	600	5.4
LM293PE4	P	PDIP	8	50	506	13.97	11230	4.32
LM393AD	D	SOIC	8	75	507	8	3940	4.32
LM393AD	D	SOIC	8	75	506.6	8	3940	4.32
LM393ADE4	D	SOIC	8	75	506.6	8	3940	4.32
LM393ADE4	D	SOIC	8	75	507	8	3940	4.32
LM393ADG4	D	SOIC	8	75	506.6	8	3940	4.32
LM393ADG4	D	SOIC	8	75	507	8	3940	4.32
LM393AP	P	PDIP	8	50	506.1	9	600	5.4
LM393AP	P	PDIP	8	50	506	13.97	11230	4.32
LM393APE4	P	PDIP	8	50	506.1	9	600	5.4
LM393APE4	P	PDIP	8	50	506	13.97	11230	4.32

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM393D	D	SOIC	8	75	507	8	3940	4.32
LM393D	D	SOIC	8	75	506.6	8	3940	4.32
LM393DE4	D	SOIC	8	75	506.6	8	3940	4.32
LM393DE4	D	SOIC	8	75	507	8	3940	4.32
LM393DG4	D	SOIC	8	75	507	8	3940	4.32
LM393DG4	D	SOIC	8	75	506.6	8	3940	4.32
LM393P	P	PDIP	8	50	506	13.97	11230	4.32
LM393P	P	PDIP	8	50	506.1	9	600	5.4
LM393PE3	P	PDIP	8	50	506.1	9	600	5.4
LM393PE4	P	PDIP	8	50	506	13.97	11230	4.32
LM393PW	PW	TSSOP	8	150	530	10.2	3600	3.5
LM393PWG4	PW	TSSOP	8	150	530	10.2	3600	3.5

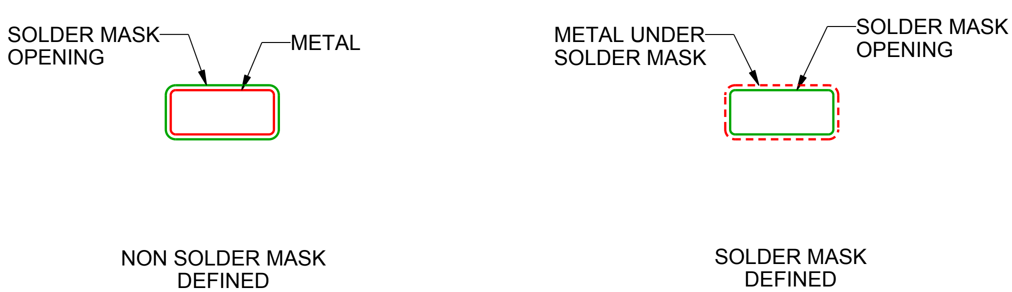


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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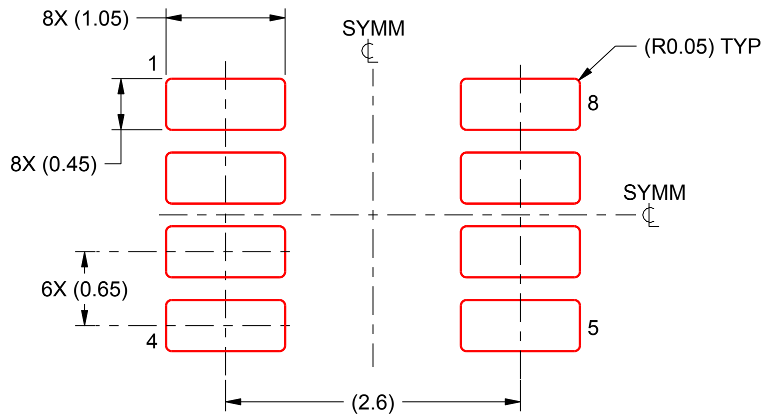
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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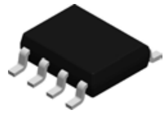
NOTES: (continued)

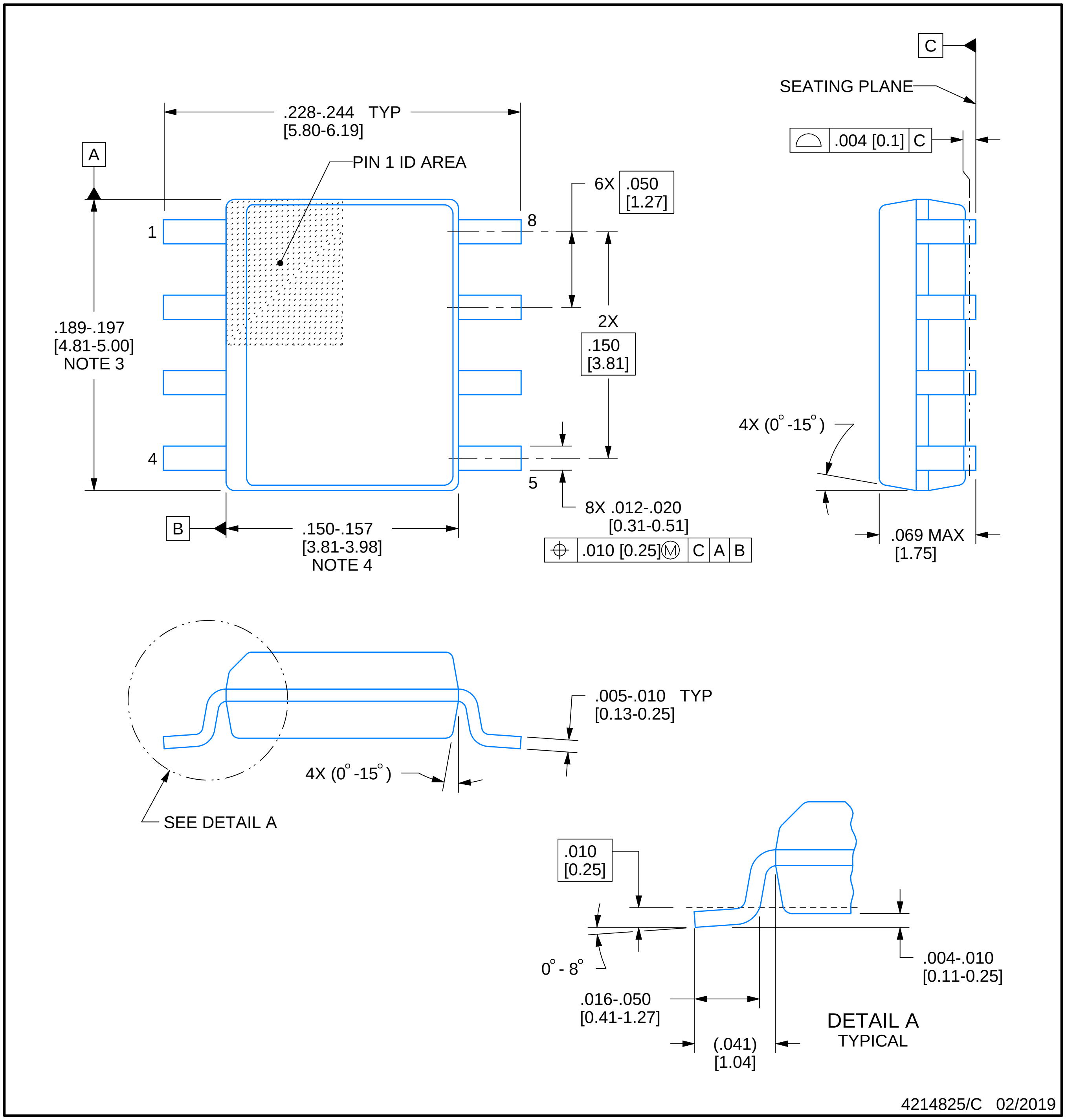
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

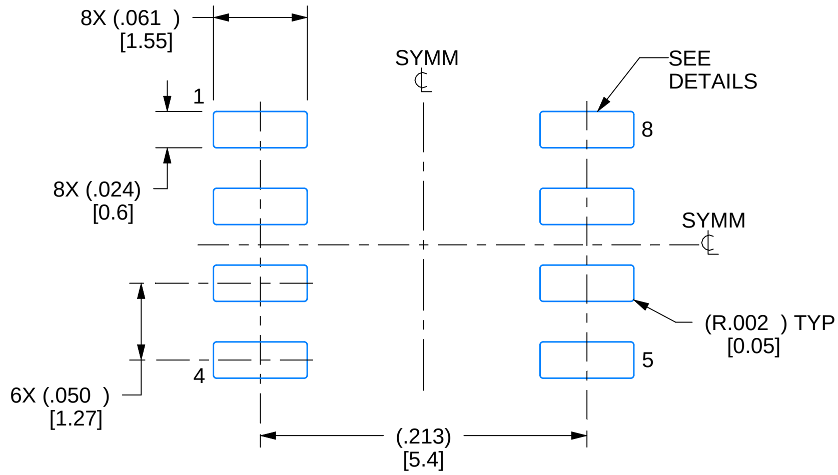
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

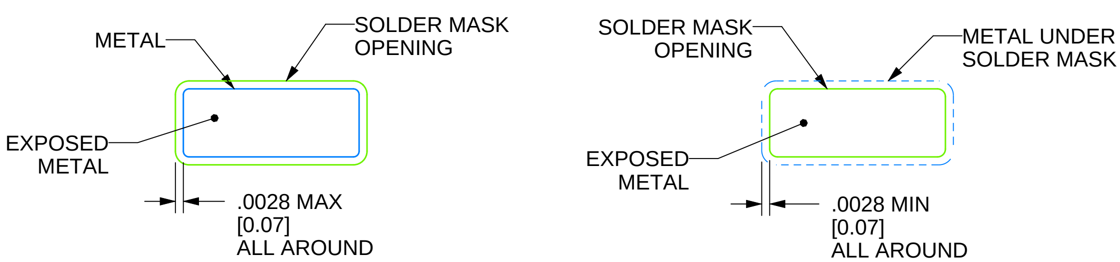


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

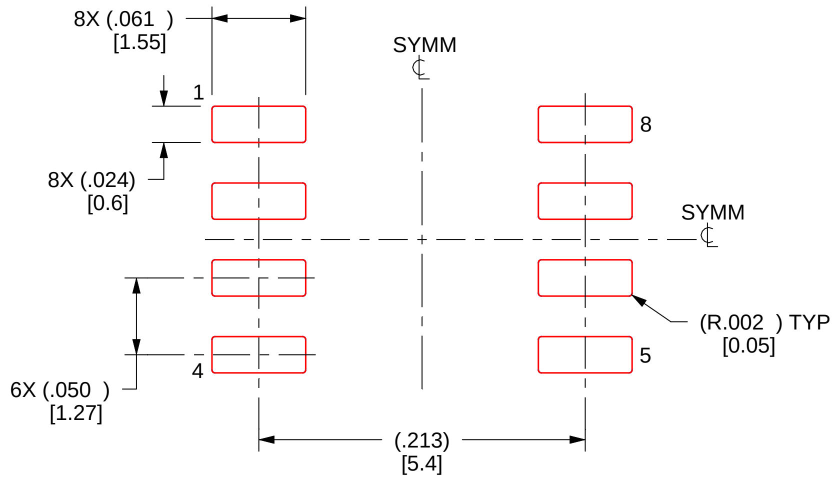
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



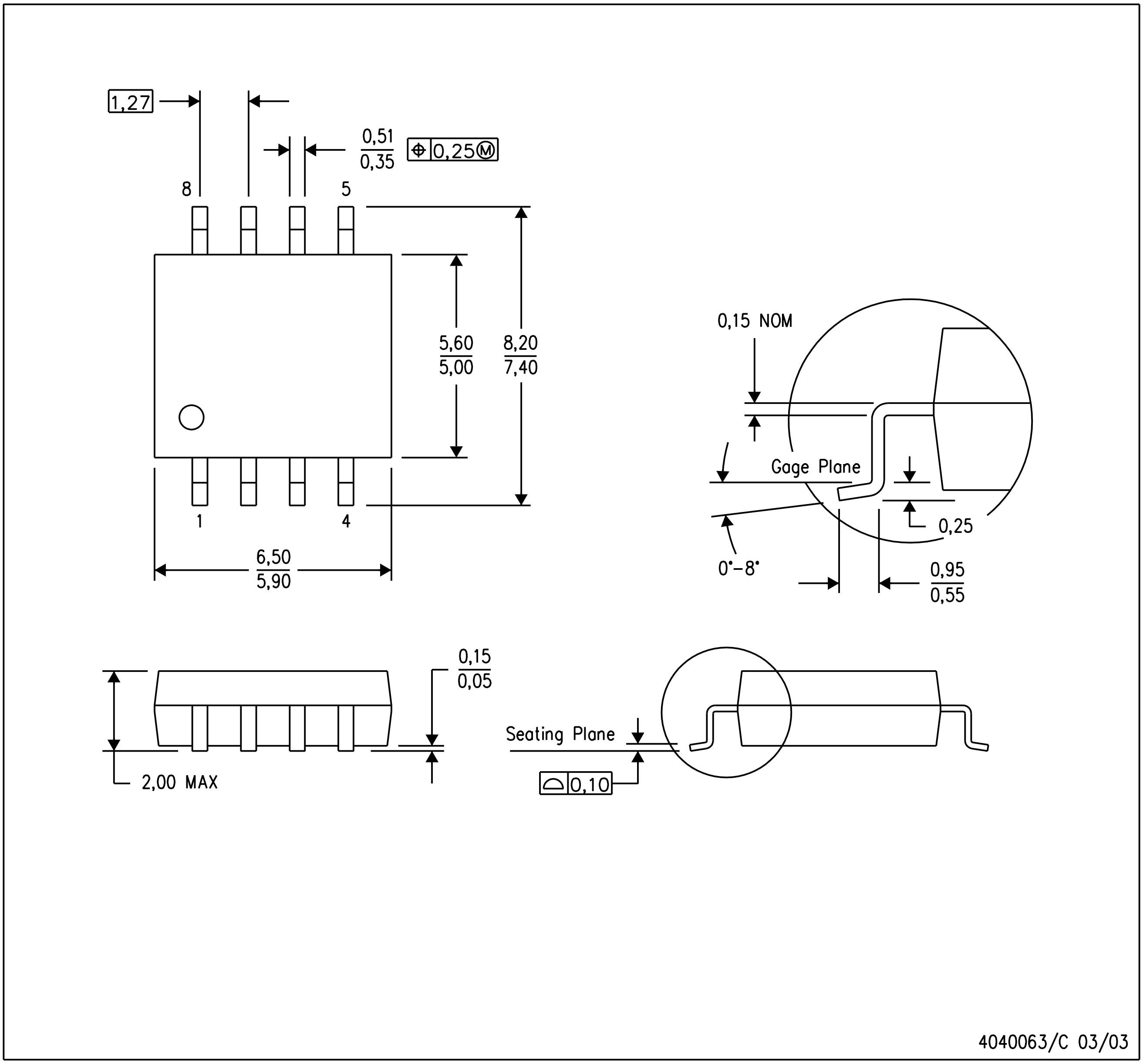
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

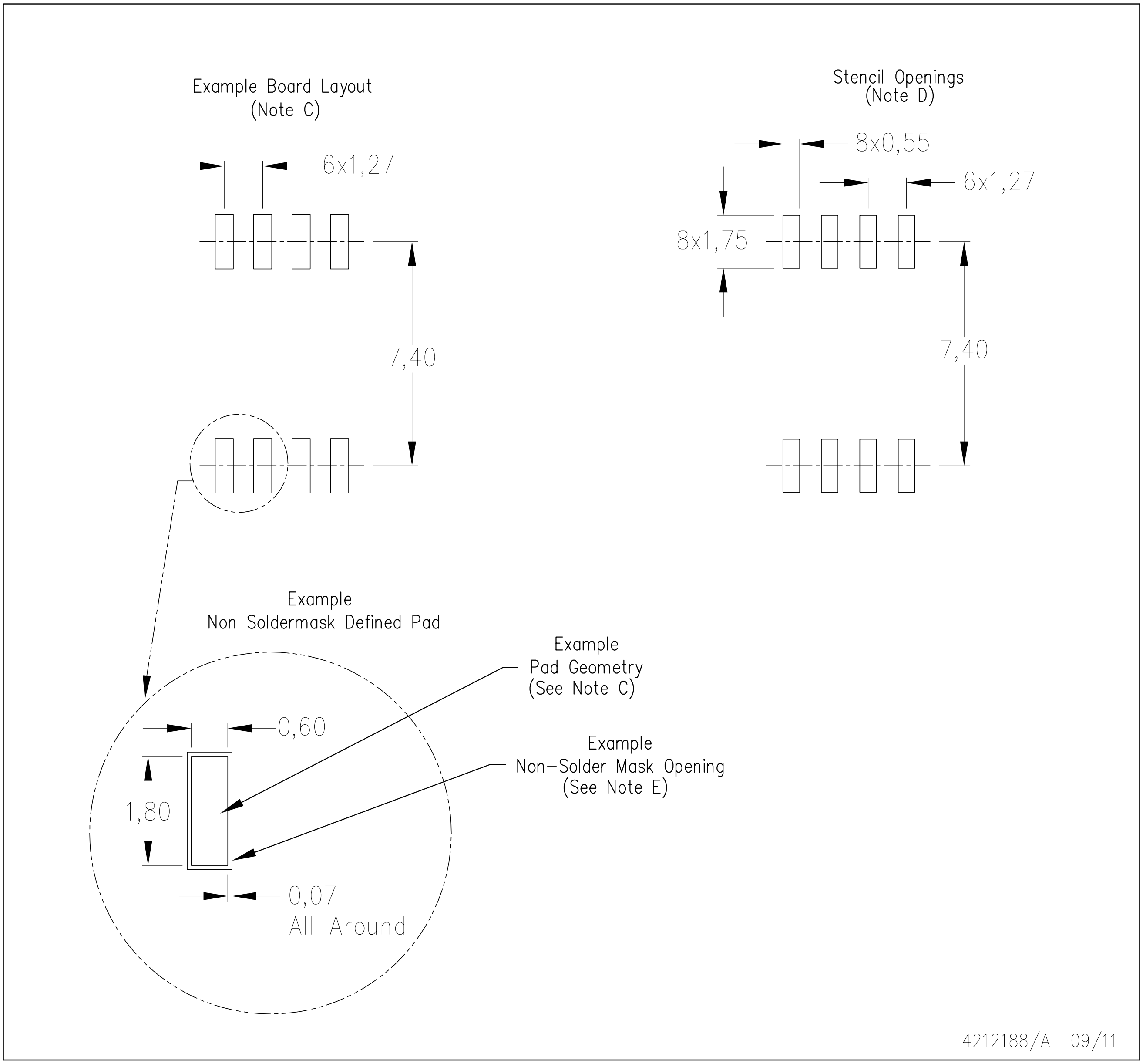
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



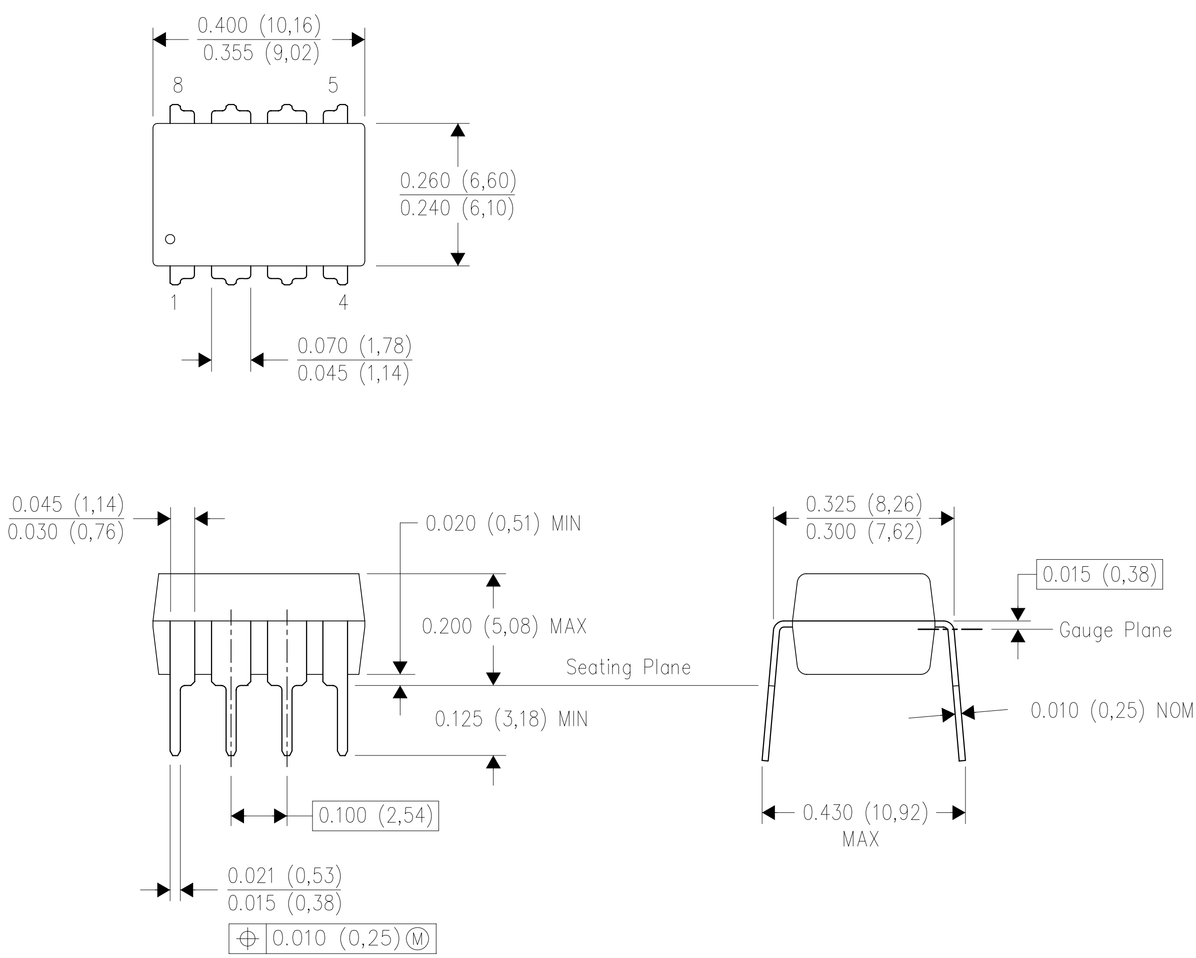
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

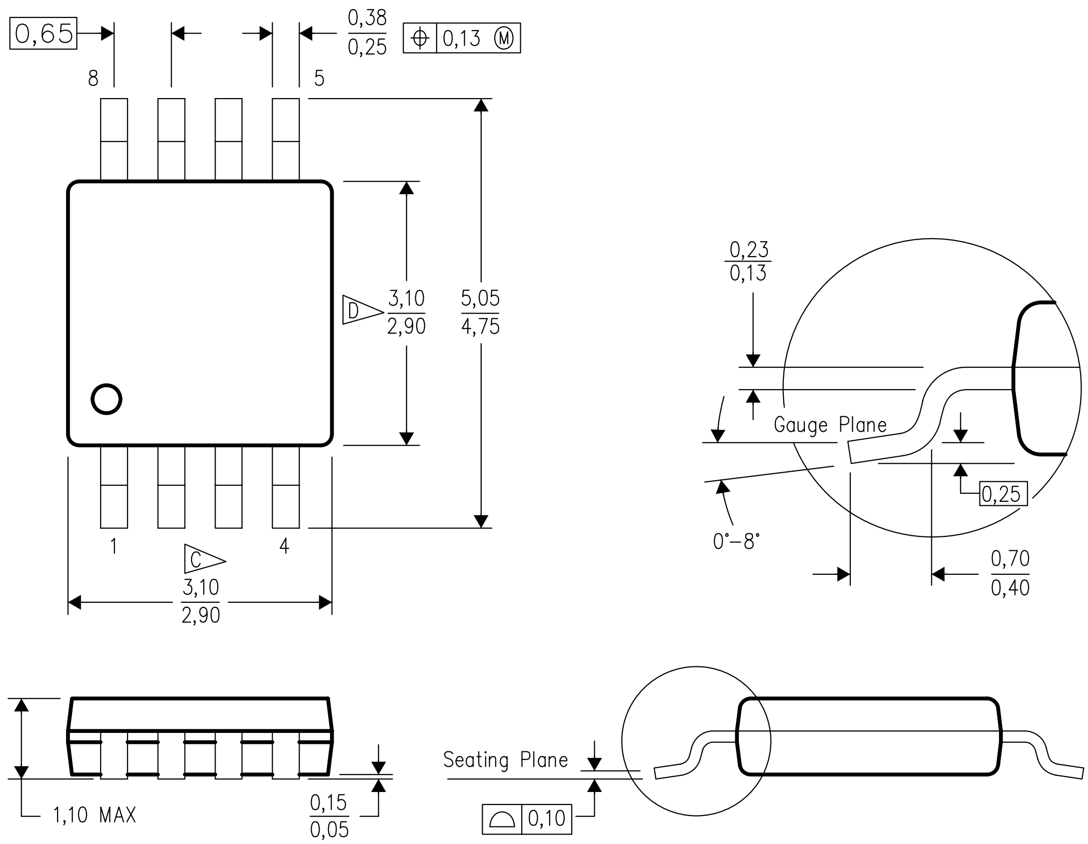
P (R-PDIP-T8) PLASTIC DUAL-IN-LINE PACKAGE



4040082/E 04/2010

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.

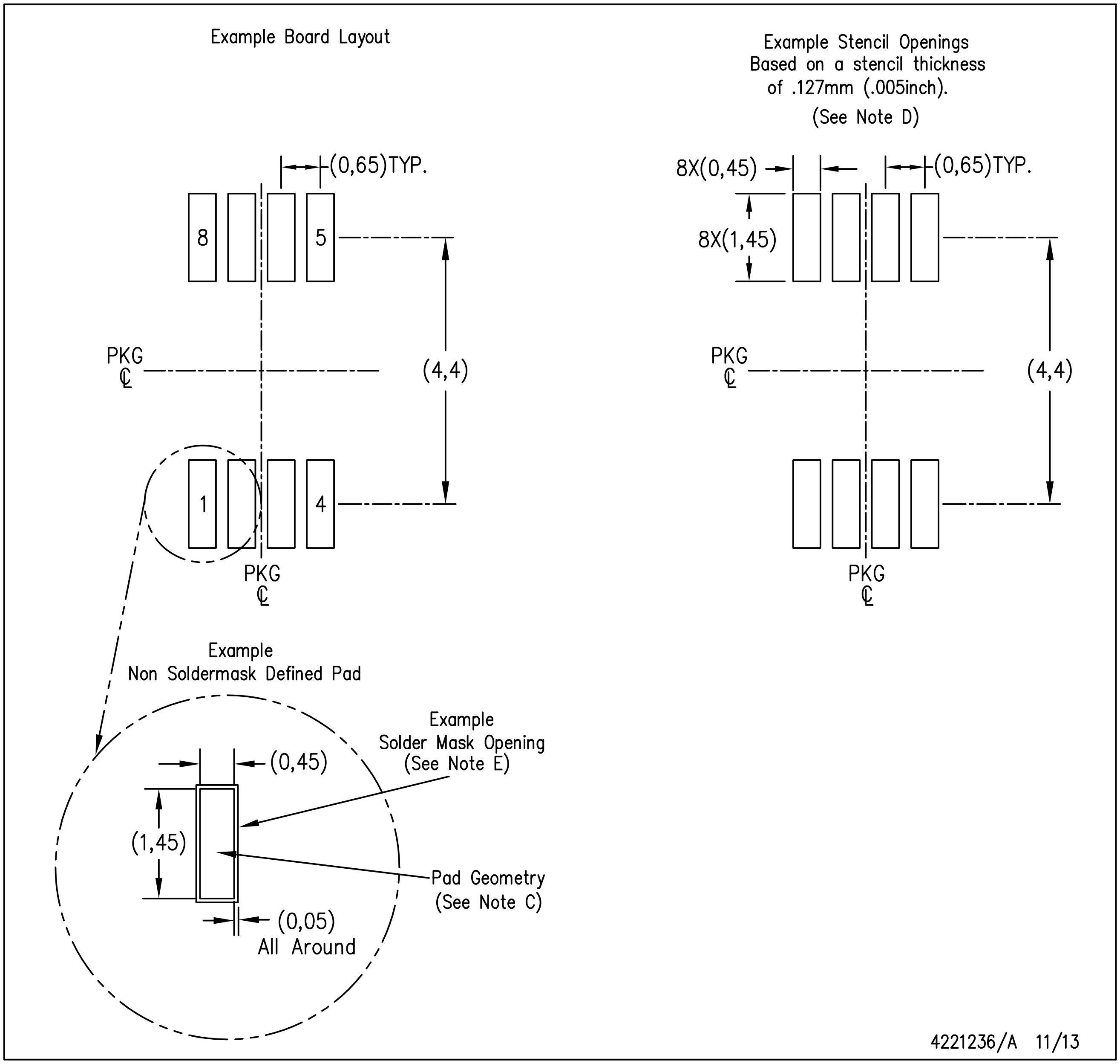
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

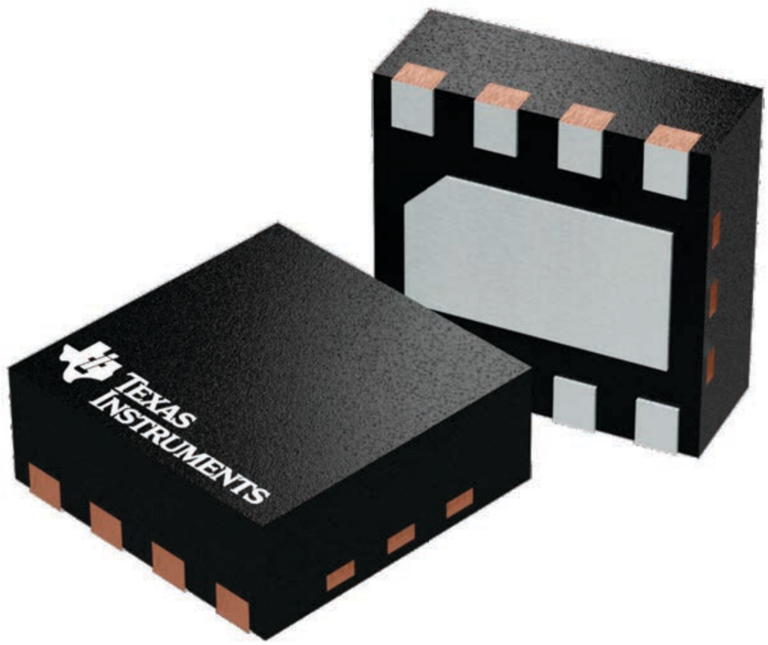
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO–187 variation AA, except interlead flash.

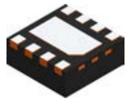
DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE

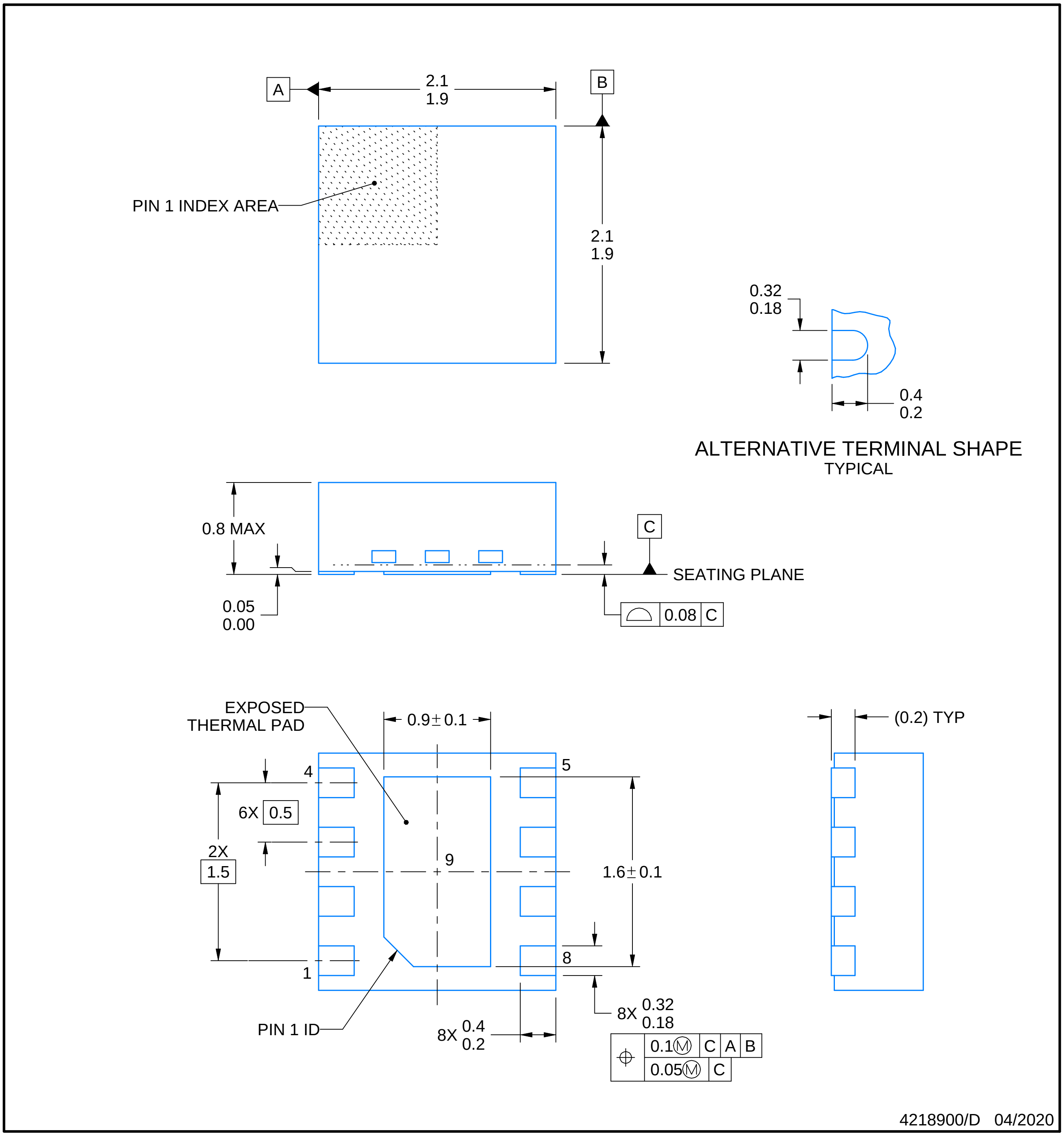


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

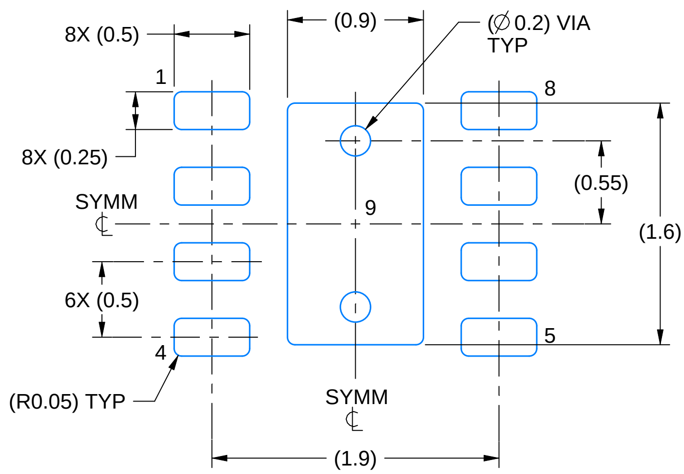




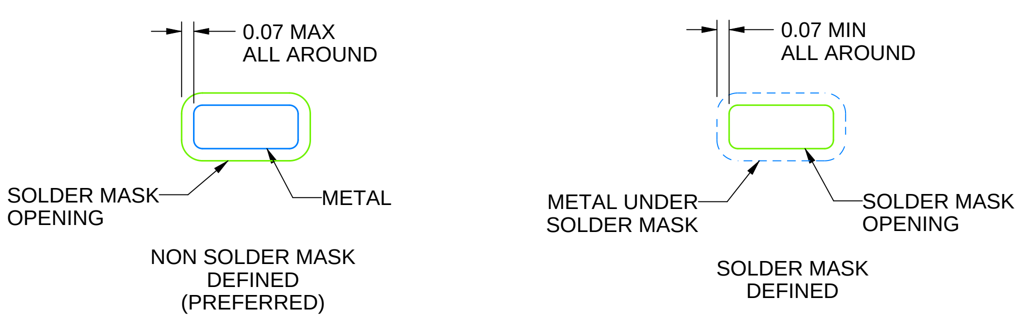


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

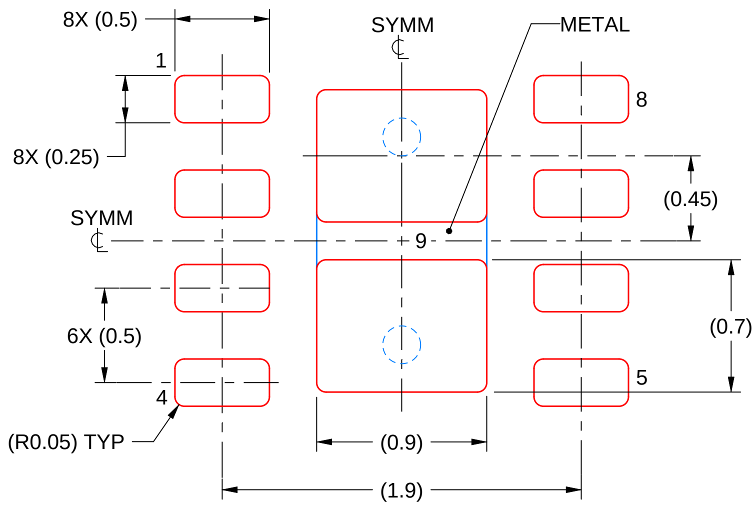


SOLDER MASK DETAILS

4218900/D 04/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



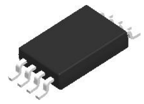
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

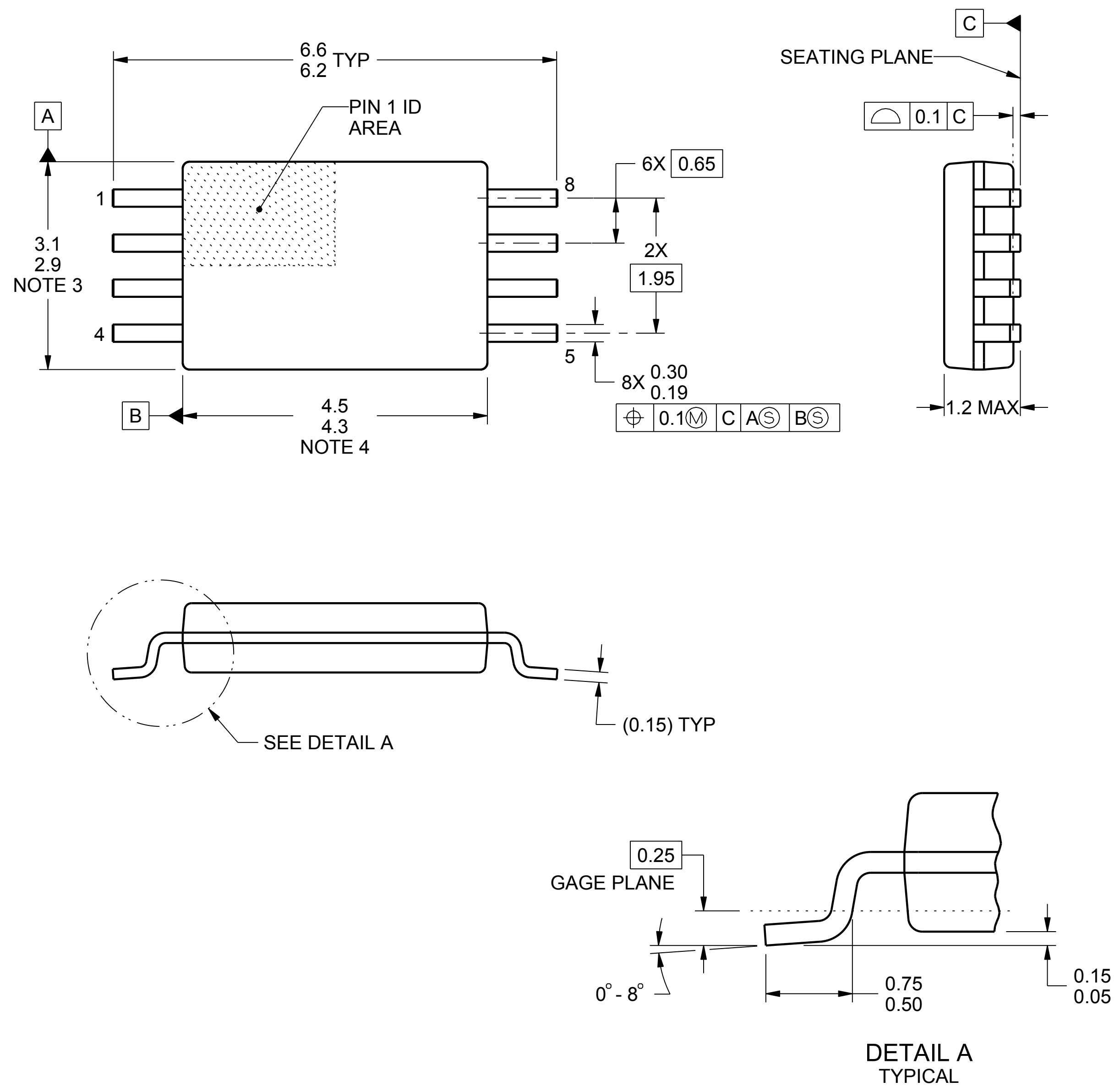
EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/D 04/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

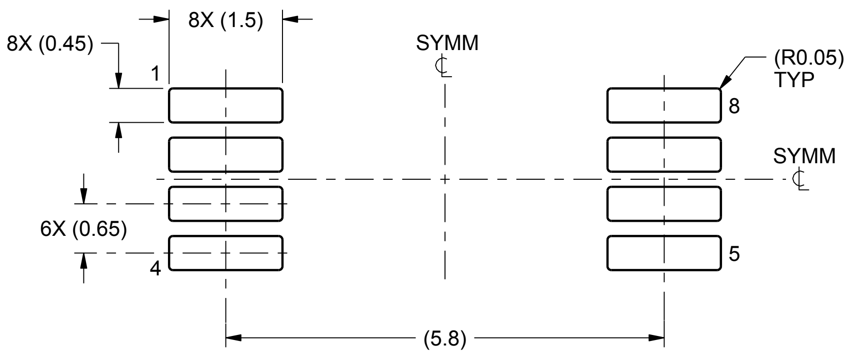




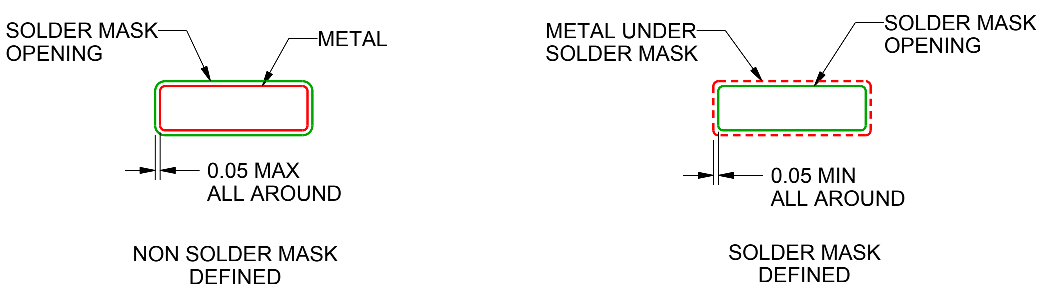
4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

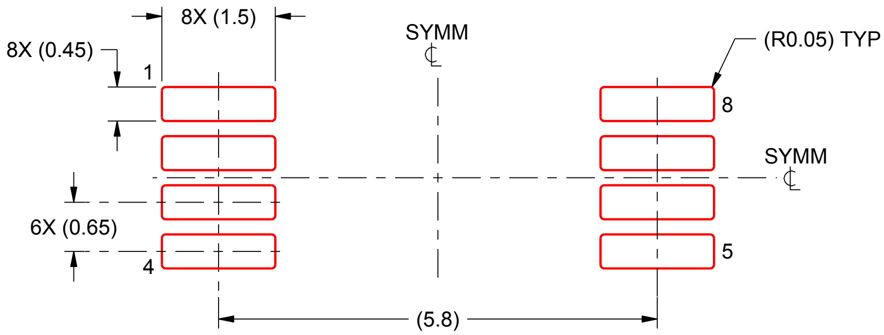


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.