SN54HC4060, SN74HC4060
14-STAGE ASYNCHRONOUS BINARY COUNTERS AND OSCILLATORS

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80-μA Max I_{CC}
- Typical t_{pd} = 14 ns
- $\pm$4-mA Output Drive at 5 V
- Low Input Current of 1 μA Max
- Allow Design of Either RC- or Crystal-Oscillator Circuits

SN54HC4060 . . . J OR W PACKAGE
SN74HC4060 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)

```
        ___
$Q_L$  [ 1    16 ]  $V_{CC}$
$Q_M$  [ 2    15 ]  $Q_J$
$Q_N$  [ 3    14 ]  $Q_H$
$Q_F$  [ 4    13 ]  $Q_I$
$Q_E$  [ 5    12 ]  CLR
$Q_G$  [ 6    11 ]  CLKI
$Q_D$  [ 7    10 ]  CLKO (overbar)
GND    [ 8     9 ]  CLKO
```

SN54HC4060 . . . FK PACKAGE
(TOP VIEW)

```
        $Q_M$ $Q_L$ NC $V_{CC}$ $Q_J$
         3    2    1   20   19
$Q_N$  [ 4              18 ]  $Q_H$
$Q_F$  [ 5              17 ]  $Q_I$
NC     [ 6              16 ]  NC
$Q_E$  [ 7              15 ]  CLR
$Q_G$  [ 8              14 ]  CLKI
         9   10   11   12   13
        $Q_D$ GND  NC  CLKO CLKO(overbar)
```

NC – No internal connection

description/ordering information

The 'HC4060 devices consist of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC- or crystal-oscillator circuits. A high-to-low transition on the clock (CLKI) input increments the counter. A high level at the clear (CLR) input disables the oscillator ($\overline{\text{CLKO}}$ goes high and CLKO goes low) and resets the counter to zero (all Q outputs low).

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP – N	Tube of 25	SN74HC4060N	SN74HC4060N
	SOIC – D	Tube of 40	SN74HC4060D	HC4060
		Reel of 2500	SN74HC4060DR	
		Reel of 250	SN74HC4060DT	
	SOP – NS	Reel of 2000	SN74HC4060NSR	HC4060
	SSOP – DB	Reel of 2000	SN74HC4060DBR	HC4060
	TSSOP – PW	Tube of 90	SN74HC4060PW	HC4060
		Reel of 2000	SN74HC4060PWR	
		Reel of 250	SN74HC4060PWT	
−55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC4060J	SNJ54HC4060J
	CFP – W	Tube of 150	SNJ54HC4060W	SNJ54HC4060W
	LCCC – FK	Tube of 55	SNJ54HC4060FK	SNJ54HC4060FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
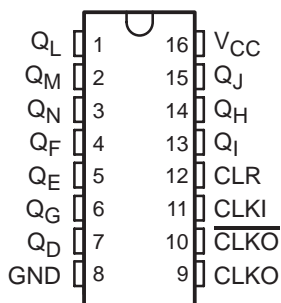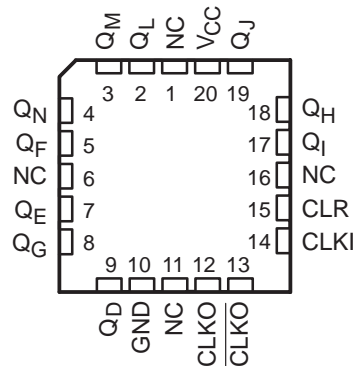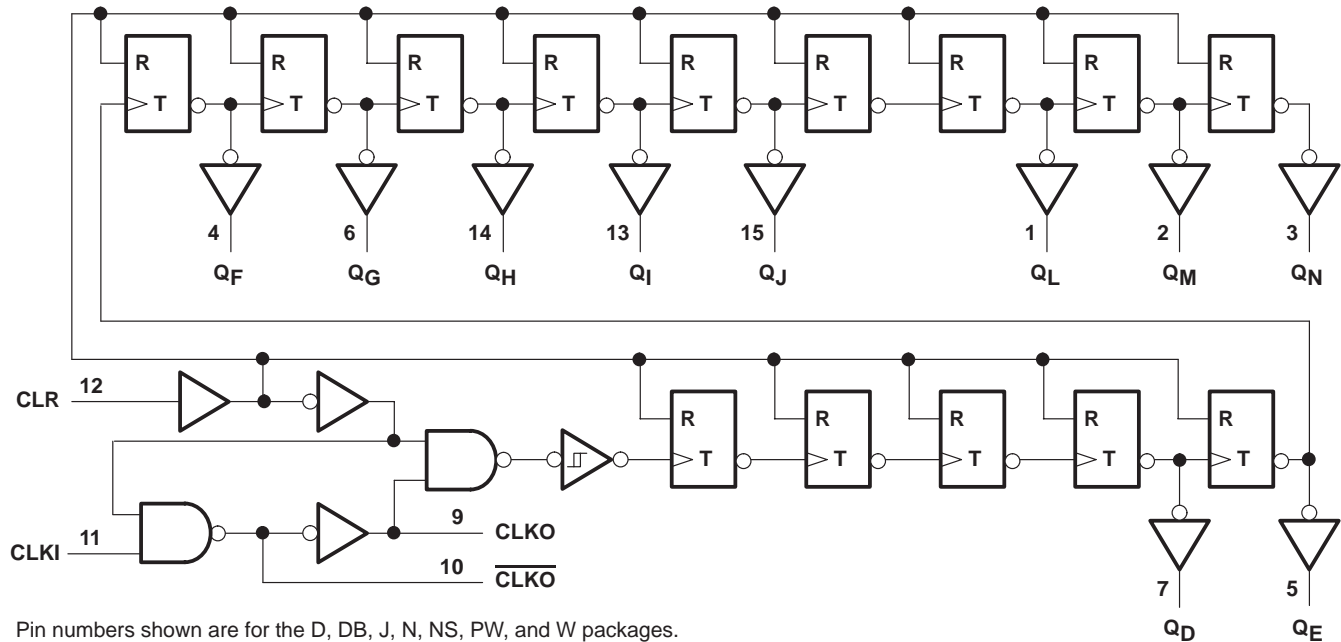
TEXAS INSTRUMENTS

SN54HC4060, SN74HC4060
14-STAGE ASYNCHRONOUS BINARY COUNTERS AND OSCILLATORS

SCLS161D – DECEMBER 1982 – REVISED SEPTEMBER 2003

FUNCTION TABLE
(each buffer)

INPUTS		FUNCTION
CLK	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L

logic diagram (positive logic)

Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) .... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) .... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... ±25 mA
Package thermal impedance, θ_{JA} (see Note 2): D package .... 73°C/W
　　　　　　　　　　　　　　　　　　　　　　　　DB package .... 82°C/W
　　　　　　　　　　　　　　　　　　　　　　　　N package .... 67°C/W
　　　　　　　　　　　　　　　　　　　　　　　　NS package .... 64°C/W
　　　　　　　　　　　　　　　　　　　　　　　　PW package .... 108°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
　　　　2. The package thermal impedance is calculated in accordance with JESD 51-7.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

recommended operating conditions (see Note 3)

			SN54HC4060			SN74HC4060			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5			1.5			V
		$V_{CC} = 4.5$ V	3.15			3.15			
		$V_{CC} = 6$ V	4.2			4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V			0.5			0.5	V
		$V_{CC} = 4.5$ V			1.35			1.35	
		$V_{CC} = 6$ V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time	$V_{CC} = 2$ V			1000			1000	ns
		$V_{CC} = 4.5$ V			500			500	
		$V_{CC} = 6$ V			400			400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	$T_A = 25°C$			SN54HC4060		SN74HC4060		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	All outputs	$V_I = V_{IH}$ or V_{IL},	$I_{OH} = -20$ μA	2 V	1.9	1.998		1.9		1.9		V
				4.5 V	4.4	4.499		4.4		4.4		
				6 V	5.9	5.999		5.9		5.9		
	Q outputs	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -4$ mA	4.5 V	3.98	4.3		3.7		3.84		
			$I_{OH} = -5.2$ mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	All outputs	$V_I = V_{IH}$ or V_{IL},	$I_{OL} = 20$ μA	2 V		0.002	0.1		0.1		0.1	V
				4.5 V		0.001	0.1		0.1		0.1	
				6 V		0.001	0.1		0.1		0.1	
	Q outputs	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 4$ mA	4.5 V		0.17	0.26		0.4		0.33	
			$I_{OL} = 5.2$ mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0			6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	$I_O = 0$		6 V			8		160		80	μA
C_i				2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	$T_A = 25°C$		SN54HC4060		SN74HC4060		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	2 V		5.5		3.7		4.3	MHz
		4.5 V		28		19		22	
		6 V		33		22		25	
t_w	Pulse duration	CLKI high or low	2 V	90		135		115	ns
			4.5 V	18		27		23	
			6 V	15		23		20	
		CLR high	2 V	90		135		115	
			4.5 V	18		27		23	
			6 V	15		23		20	
t_{su}	Setup time, CLR inactive before CLKI↓	2 V	160		240		200		ns
		4.5 V	32		48		40		
		6 V	27		41		34		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25°C$			SN54HC4060		SN74HC4060		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	5.5	10		3.7		4.3		MHz
			4.5 V	28	45		19		22		
			6 V	33	53		22		25		
t_{pd}	CLKI	Q_D	2 V		240	490		735		615	ns
			4.5 V		58	98		147		123	
			6 V		42	83		125		105	
t_{PHL}	CLR	Any Q	2 V		66	140		210		175	ns
			4.5 V		18	28		42		35	
			6 V		14	24		36		30	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	30		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	88	pF

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

VOLTAGE WAVEFORMS
SETUP AND INPUT RISE AND FALL TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

VOLTAGE WAVEFORMS
PULSE DURATIONS
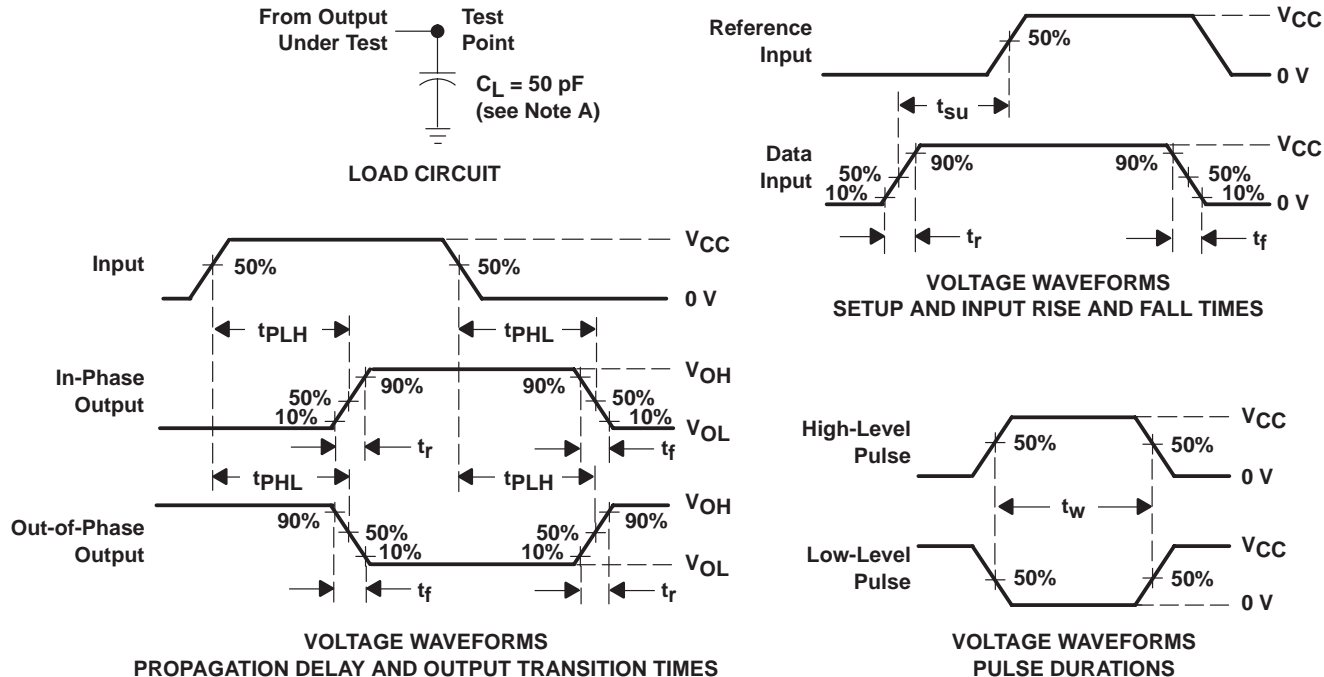
NOTES: A. C_L includes probe and test-fixture capacitance.
　　　　B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
　　　　C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
　　　　D. The outputs are measured one at a time with one input transition per measurement.
　　　　E. t_{PLH} and t_{PHL} are the same as t_{pd}.

**Figure 1. Load Circuit and Voltage Waveforms**

CONNECTING AN RC-OSCILLATOR CIRCUIT TO THE 'HC4060 DEVICES

The 'HC4060 devices consist of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC- or crystal-oscillator circuits.

When an RC-oscillator circuit is implemented, two resistors and a capacitor are required. The components are attached to the terminals as shown:
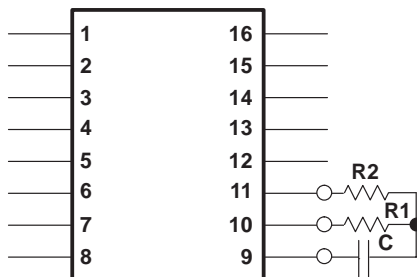
To determine the values of capacitance and resistance necessary to obtain a specific oscillator frequency (f), use this formula:

$$f = \frac{1}{2(R1)(C)\left(\frac{0.405\,R2}{R1+R2} + 0.693\right)}$$

If R2 > > R1 (i.e., R2 = 10R1), the above formula simplifies to:

$$f = \frac{0.455}{RC}$$

PACKAGING INFORMATION

Orderable Device (1)	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN54HC4060FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HC 4060FK	Samples
SN74HC4060D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4060	Samples
SN74HC4060DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4060	Samples
SN74HC4060DBRG4	ACTIVE	SSOP	DB	16	2000	TBD	Call TI	Call TI	-40 to 85		Samples
SN74HC4060DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4060	Samples
SN74HC4060DT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4060	Samples
SN74HC4060N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC4060N	Samples
SN74HC4060NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4060	Samples
SN74HC4060NSRE4	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4060	Samples
SN74HC4060PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4060	Samples
SN74HC4060PWG4	ACTIVE	TSSOP	PW	16	90	TBD	Call TI	Call TI	-40 to 85		Samples
SN74HC4060PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	SN	Level-1-260C-UNLIM	-40 to 85	HC4060	Samples
SN74HC4060PWRE4	ACTIVE	TSSOP	PW	16	2000	TBD	Call TI	Call TI	-40 to 85		Samples
SN74HC4060PWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4060	Samples
SN74HC4060PWT	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4060	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54HC4060, SN74HC4060 :

- Catalog : SN74HC4060

- Automotive : SN74HC4060-Q1, SN74HC4060-Q1

- Military : SN54HC4060

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

● Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC4060DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74HC4060DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC4060DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC4060NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC4060PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC4060PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC4060PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC4060PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC4060DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74HC4060DR	SOIC	D	16	2500	356.0	356.0	35.0
SN74HC4060DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74HC4060NSR	SO	NS	16	2000	356.0	356.0	35.0
SN74HC4060PWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74HC4060PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC4060PWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC4060PWT	TSSOP	PW	16	250	356.0	356.0	35.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN54HC4060FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SN74HC4060D	D	SOIC	16	40	506.6	8	3940	4.32
SN74HC4060D	D	SOIC	16	40	507	8	3940	4.32
SN74HC4060N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC4060N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC4060PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74HC4060PWG4	PW	TSSOP	16	90	530	10.2	3600	3.5

FK (S−CQCC−N**)   LEADLESS CERAMIC CHIP CARRIER
28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

$\dfrac{0.020\ (0,51)}{0.010\ (0,25)}$

$\dfrac{0.020\ (0,51)}{0.010\ (0,25)}$

$\dfrac{0.080\ (2,03)}{0.064\ (1,63)}$

$\dfrac{0.055\ (1,40)}{0.045\ (1,14)}$

$\dfrac{0.045\ (1,14)}{0.035\ (0,89)}$

$\dfrac{0.028\ (0,71)}{0.022\ (0,54)}$

0.050 (1,27)

$\dfrac{0.045\ (1,14)}{0.035\ (0,89)}$

4040140/D 01/11

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   This package can be hermetically sealed with a metal lid.
          D.   Falls within JEDEC MS−004
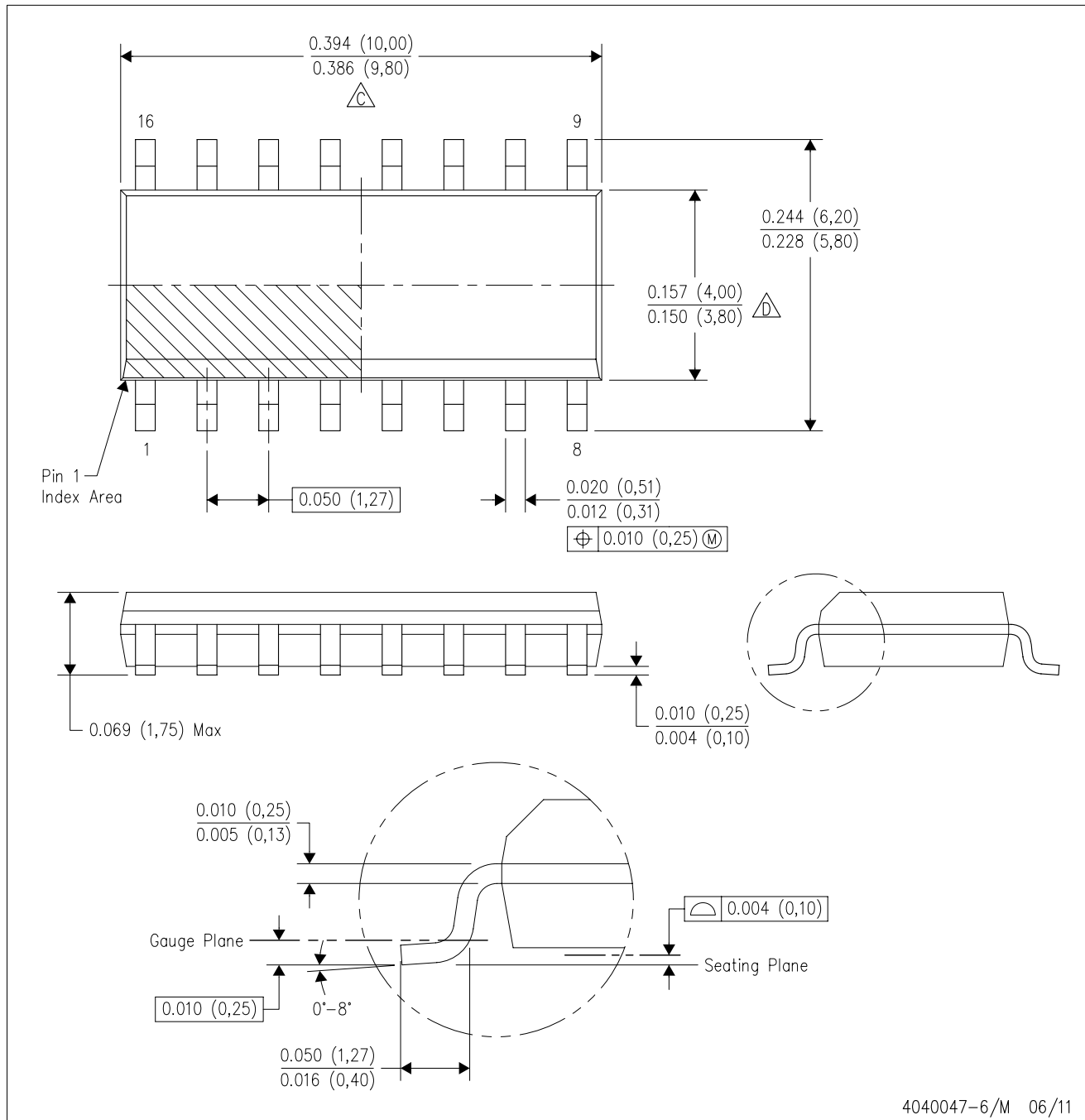
TEXAS INSTRUMENTS
www.ti.com

D (R−PDSO−G16) PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
⚠C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⚠D

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M 06/11

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
⚠C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
not exceed 0.006 (0,15) each side.
⚠D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS−012 variation AC.

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE
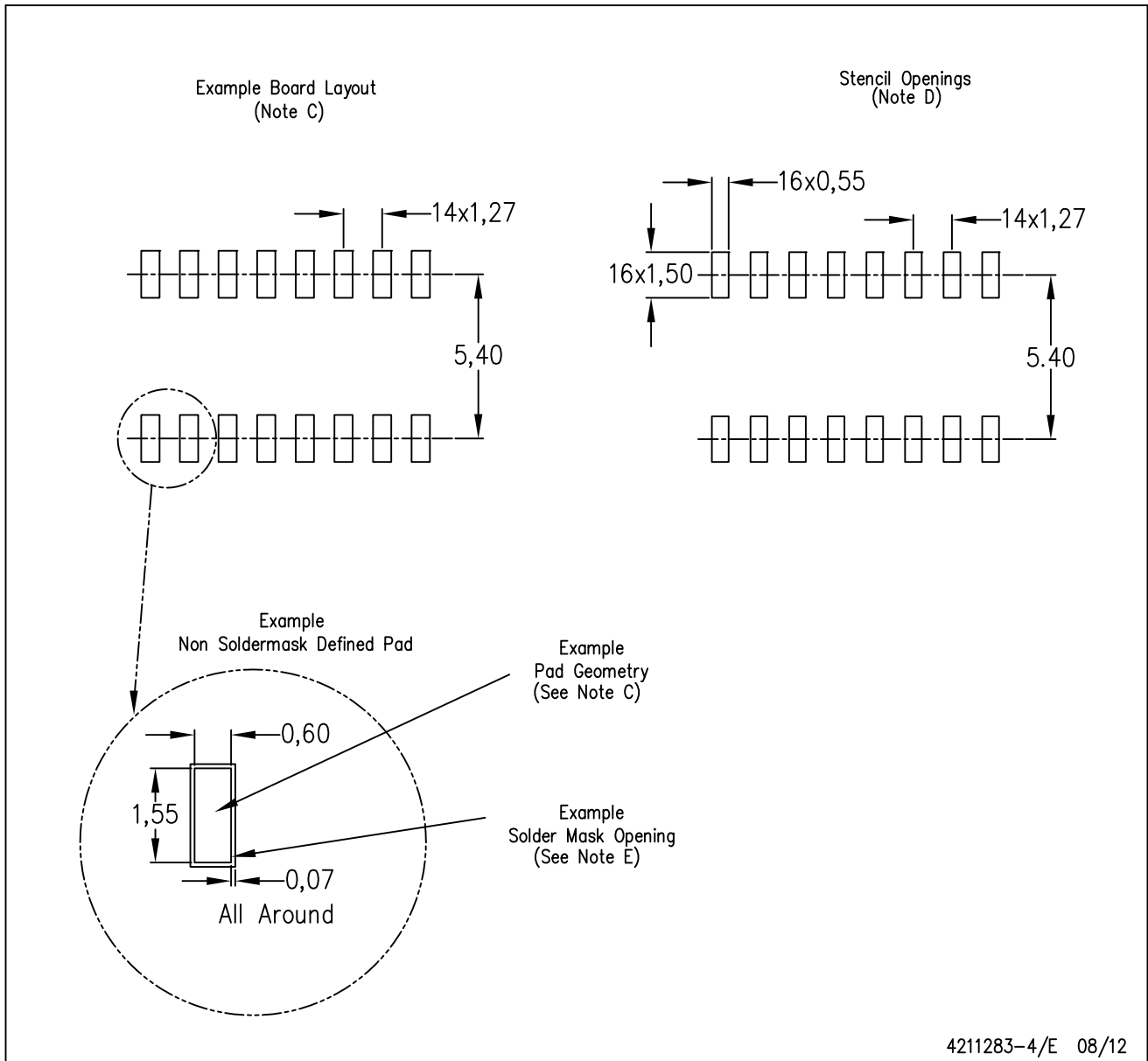
Example Board Layout
(Note C)

Stencil Openings
(Note D)

14x1,27

16x0,55

14x1,27

16x1,50

5,40

5.40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0,07

All Around

4211283−4/E 08/12

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate designs.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

6.6
6.2 TYP

A

PIN 1 INDEX AREA

14X 0.65

16

SEATING PLANE

C

△ 0.1 C

1

2X

4.55

5.1
4.9
NOTE 3

8

9

16X 0.30
0.19

⊕ 0.1 Ⓜ C A B

B

4.5
4.3
NOTE 4

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25
GAGE PLANE

0.15
0.05

0°-8°

0.75
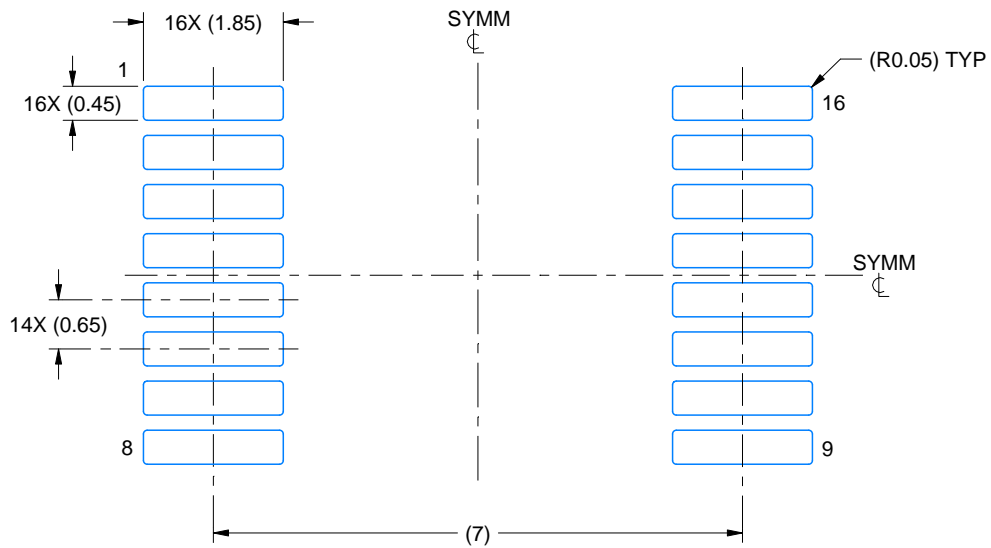0.50

DETAIL A
TYPICAL

4220204/A   02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220204/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PW0016A

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

8.2 / 7.4 TYP

A

PIN 1 INDEX AREA

1

16

14X 0.65

2X

4.55

6.5 / 5.9 NOTE 3

8

9

16X 0.38 / 0.22

B

5.6 / 5.0 NOTE 4

⊕ 0.1 Ⓜ C A B

C

⌒ 0.1 C

SEATING PLANE

0.25 / 0.09

SEE DETAIL A

0.25

GAGE PLANE

2 MAX

0°-8°

0.95 / 0.55

0.05 MIN

DETAIL A
TYPICAL
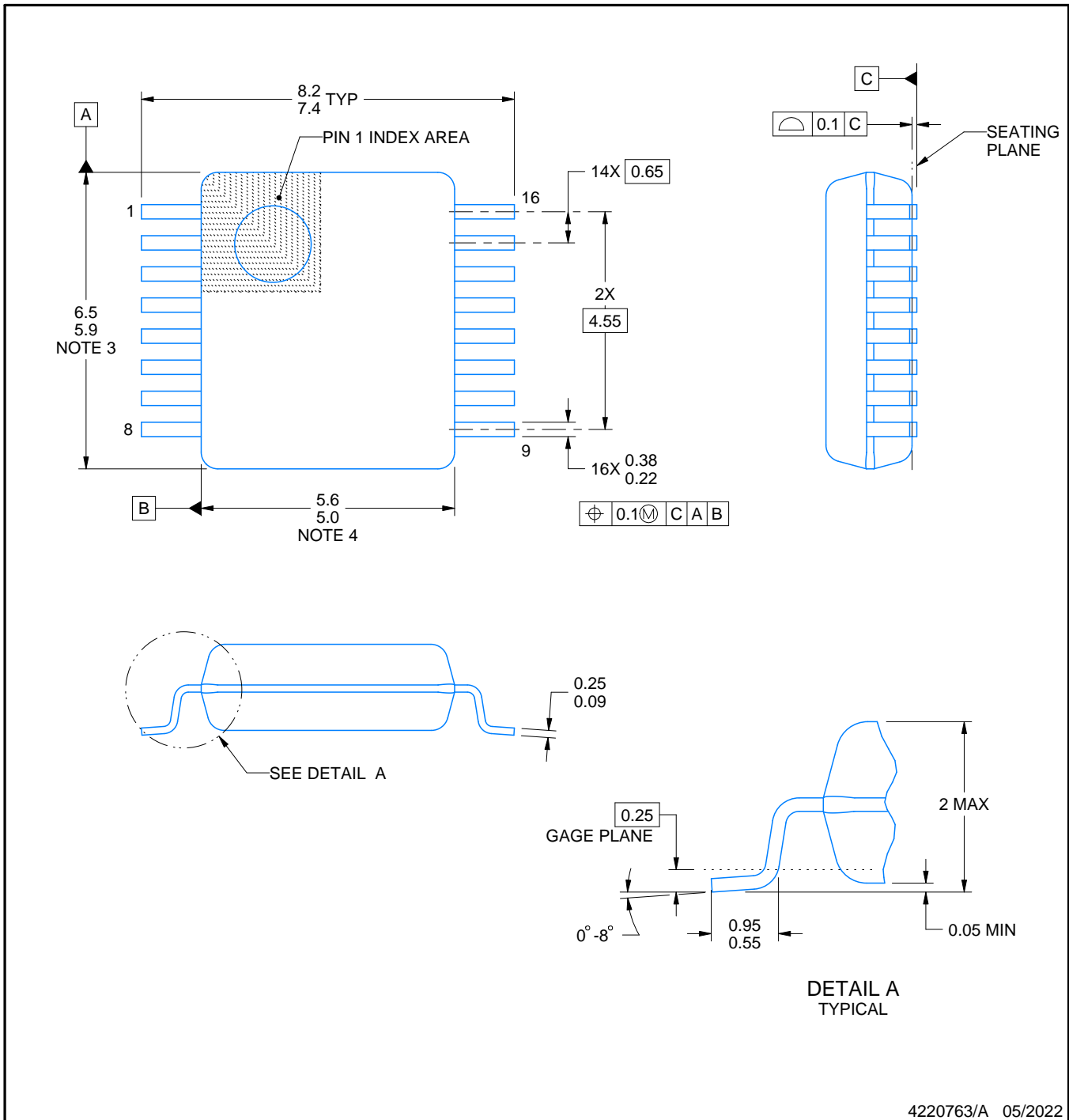
4220763/A   05/2022
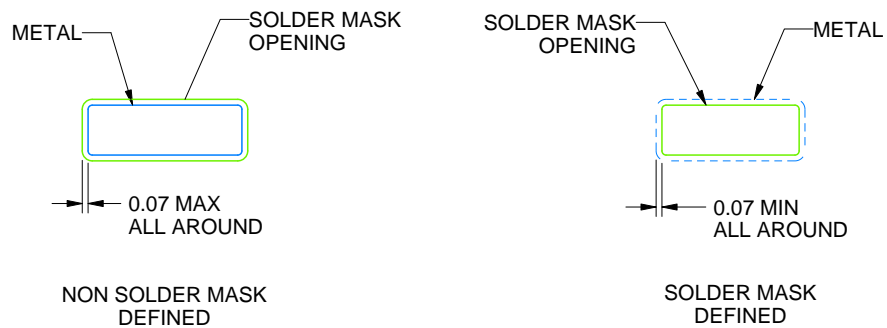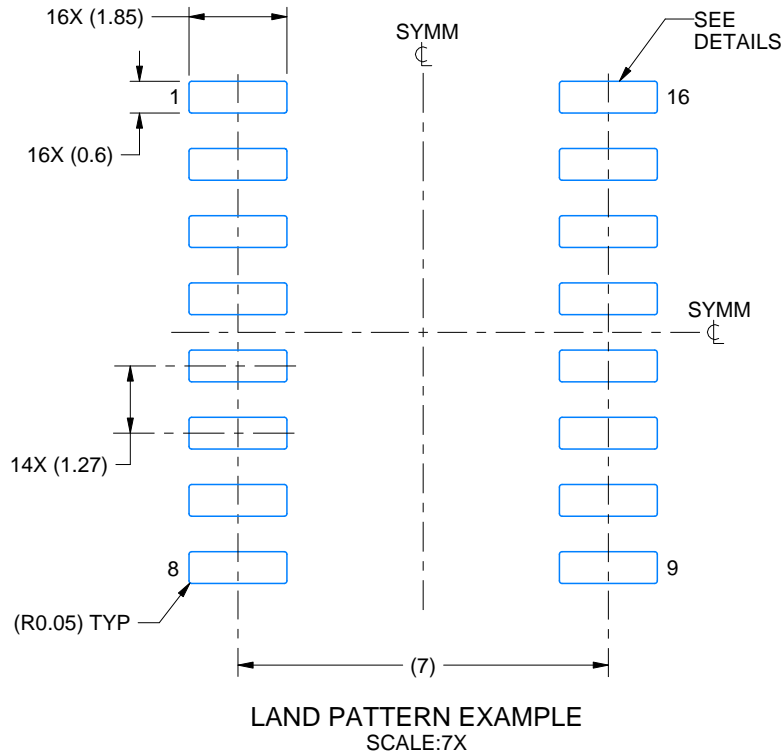
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

DB0016A

16X (1.85)

1

16X (0.45)

14X (0.65)

8

SYMM

(R0.05) TYP

16

SYMM

9

(7)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220763/A   05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.85)

1

16X (0.45)

14X (0.65)

8

SYMM

(R0.05) TYP

16

SYMM

9

(7)
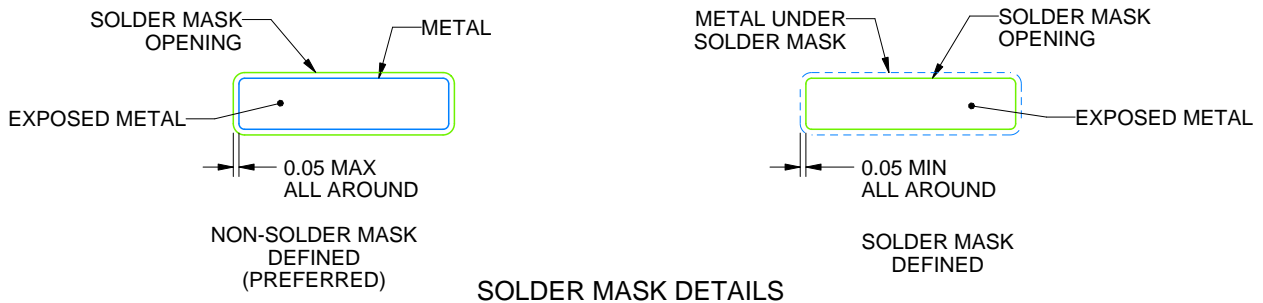
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A   05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
B.   This drawing is subject to change without notice.
C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R−PDIP−T**)

PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14)   △D

0.045 (1,14)   △D
0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)
Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.010 (0,25) NOM

0.125 (3,18) MIN

0.100 (2,54)

0.430 (10,92) MAX

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option   △D

4040049/E   12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
      △C   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
      △D   The 20 pin end lead shoulder width is a vendor option, either half or full width.
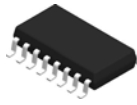
TEXAS
INSTRUMENTS
www.ti.com
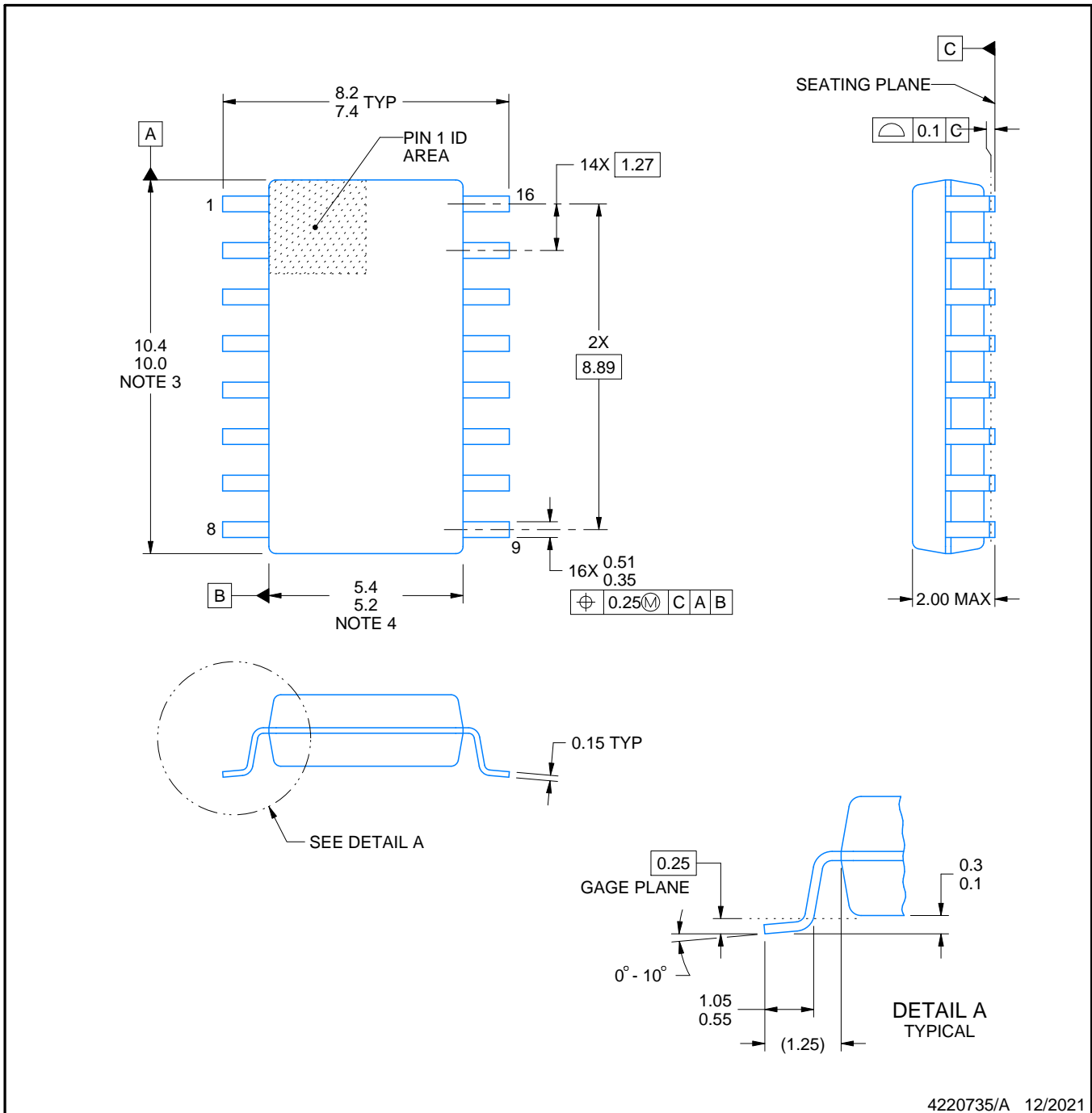
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

16X (1.85)

SYMM
℄

SEE
DETAILS

1

16

16X (0.6)

SYMM
℄

14X (1.27)

8

9

(R0.05) TYP

(7)

LAND PATTERN EXAMPLE
SCALE:7X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A   12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.85)

SYMM
℄

1

16X (0.6)

16

SYMM
℄

14X (1.27)

8

9

(R0.05) TYP

(7)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A   12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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