SNx4HC541 具有三态输出的八路缓冲器和线路驱动器

1 特性

- 2V 至 6V 的宽工作电压范围
- 高电流三态输出直接驱动总线或多达 15 个 LSTTL 负载
- 低功耗，I_{CC} 最大值为 80μA
- t_{pd} 典型值 = 10 ns
- ±6mA 输出驱动（电压为 5V 时）
- 低输入电流，最大值为 1μA
- 数据直通式引脚排列（所有输入均在输出对侧）

2 应用

- LED
- 服务器
- PC 和笔记本电脑
- 可穿戴健康设备
- 电子销售终端

3 说明

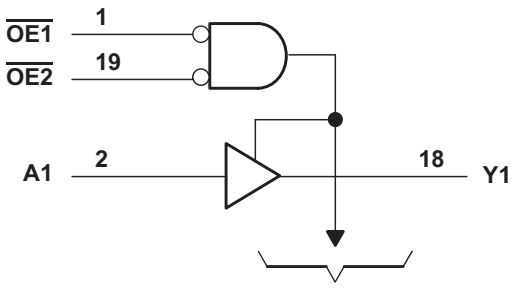
这些八路缓冲器和线路驱动器具有 SNx4HC541 器件的性能，以及封装两侧输入和输出的引脚排列。这种布置非常有助于印刷电路板布局布线。

三态输出由双输入或非门控制。如果任一输出使能端（$\overline{OE1}$ 或 $\overline{OE2}$）输入为高电平，则所有八路输出均处于高阻抗状态。SNx4HC541 器件在输出端提供真实数据。

器件信息

器件型号	封装[1]	封装尺寸（标称值）
SN74HC541DW	SOIC (20)	12.80mm × 7.50mm
SN74HC541DB	SSOP (20)	7.20mm × 5.30mm
SN74HC541N	PDIP (20)	24.33mm × 6.35mm
SN74HC541NS	SO (20)	12.60mm × 5.30mm
SN74HC541PW	TSSOP (20)	6.50mm × 4.40mm
SN54HC541J	CDIP (20)	24.20mm × 6.92mm
SN54HC541FK	LCCC (20)	8.89mm × 8.89mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



功能方框图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

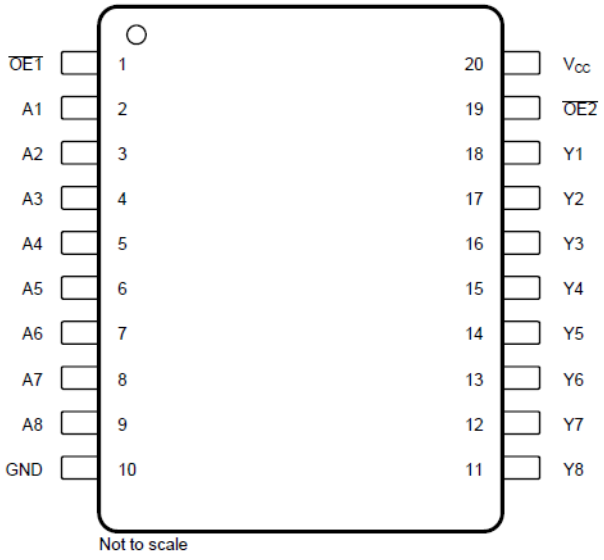
Changes from Revision D (September 2016) to Revision E (May 2022) — **Page**

- Updated ESD ratings table to include modern TI terminology ... 4
- Junction-to-ambient thermal resistance values increased. DB was 90.2 is now 122.7, DW was 77.5 is now 109.1, N was 45.2 is now 84.6, NS was 72.8 is now 113.4, PW was 98.3 is now 131.8 ... 5

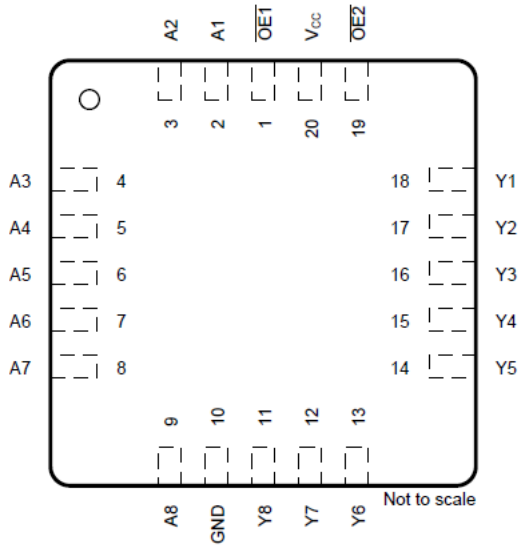
Changes from Revision C (August 2003) to Revision D (September 2016) — **Page**

- 添加了*应用* 部分、*热性能信息* 表、*ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1
- 删除了*订购信息* 表，请参阅数据表末尾的*机械、封装和可订购信息* ... 1
- Changed $R_{\theta JA}$ for DB package from 70°C/W: to 90.2°C/W ... 5
- Changed $R_{\theta JA}$ for DW package from 58°C/W: to 77.5°C/W ... 5
- Changed $R_{\theta JA}$ for N package from 69°C/W: to 45.2°C/W ... 5
- Changed $R_{\theta JA}$ for NS package from 60°C/W: to 72.8°C/W ... 5
- Changed $R_{\theta JA}$ for PW package from 83°C/W: to 98.3°C/W ... 5

5 Pin Configuration and Functions



DB, DW, N, NS, J, or PW Package
20-Pin SSOP, SOIC, PDIP, SO, CDIP, or TSSOP
Top View



FK Package
20-Pin LCCC
Top View

Pin Functions

PIN		I/O[1]	DESCRIPTION
NO.	NAME		
1	$\overline{OE1}$	I	Output enable (active low) Both $\overline{OE}$ must be low to enable outputs
2	A1	I	Channel 1 input
3	A2	I	Channel 2 input
4	A3	I	Channel 3 input
5	A4	I	Channel 4 input
6	A5	I	Channel 5 input
7	A6	I	Channel 6 input
8	A7	I	Channel 7 input
9	A8	I	Channel 8 input
10	GND	—	Ground
11	Y8	O	Channel 8 output
12	Y7	O	Channel 7 output
13	Y6	O	Channel 6 output
14	Y5	O	Channel 5 output
15	Y4	O	Channel 4 output
16	Y3	O	Channel 3 output
17	Y2	O	Channel 2 output
18	Y1	O	Channel 1 output
19	$\overline{OE2}$	I	Output enable (active low) both $\overline{OE}$ must be low to enable outputs
20	V_{CC}	—	Power pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See note(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 6 V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise and fall time	V_{CC} = 2 V			1000	ns
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature	SN54HC541	–55		125	°C
		SN74HC541	–40		85	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC		SN74HC541					UNIT
		DB (SSOP)	DW (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)	
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[1]	122.7	109.1	84.6	113.4	131.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	81.6	76	72.5	78.6	72.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.5	77.6	65.3	78.4	82.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	46.1	51.5	55.3	47.1	21.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	77.1	77.1	65.2	78.1	82.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics, T_A = 25°C

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 µA	2 V	1.9	1.998		V
			4.5 V	4.4	4.499		
			6 V	5.9	5.999		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	2 V	0.002		0.1	V
			4.5 V	0.001		0.1	
			6 V	0.001		0.1	
		I_{OL} = 6 mA	4.5 V	0.17		0.26	
		I_{OL} = 7.8 mA	6 V	0.15		0.26	
I_I	$V_I = V_{CC}$ or 0		6 V	±0.1		±100	nA
I_{OZ}	$V_O = V_{CC}$ or 0		6 V	±0.01		±0.5	µA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0		6 V			8	µA
C_i			2 V to 6 V		3	10	pF

6.6 Electrical Characteristics, SN54HC541

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 µA	2 V	1.9			V
			4.5 V	4.4			
			6 V	5.9			
		I_{OH} = –6 mA	4.5 V	3.7			
		I_{OH} = –7.8 mA	6 V	5.2			

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	2 V			0.1	V
			4.5 V			0.1	
			6 V			0.1	
		I_{OL} = 6 mA	4.5 V			0.4	
		I_{OL} = 7.8 mA	6 V			0.4	
I_I	$V_I = V_{CC}$ or 0		6 V			±1000	nA
I_{OZ}	$V_O = V_{CC}$ or 0		6 V			±10	μA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0		6 V			160	μA
C_i			2 V to 6 V			10	pF

6.7 Electrical Characteristics, SN74HC541

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = – 20 μA	2 V	1.9			V
			4.5 V	4.4			
			6 V	5.9			
		I_{OH} = – 6 mA	4.5 V	3.84			
		I_{OH} = – 7.8 mA	6 V	5.34			
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	2 V			0.1	V
			4.5 V			0.1	
			6 V			0.1	
		I_{OL} = 6 mA	4.5 V			0.33	
		I_{OL} = 7.8 mA	6 V			0.33	
I_I	$V_I = V_{CC}$ or 0		6 V			±1000	nA
I_{OZ}	$V_O = V_{CC}$ or 0		6 V			±5	μA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0		6 V			80	μA
C_i			2 V to 6 V			10	pF

6.8 Switching Characteristics, C_L = 50 pF, T_A = 25°C

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	2 V		40	115	ns
			4.5 V		12	23	
			6 V		10	20	
t_{en}	$\overline{OE}$	Y	2 V		80	150	ns
			4.5 V		17	30	
			6 V		15	26	
t_{dis}	$\overline{OE}$	Y	2 V		40	150	ns
			4.5 V		18	30	
			6 V		17	26	
t_t		Y	2 V		28	60	ns
			4.5 V		8	12	
			6 V		6	10	

6.9 Switching Characteristics, C_L = 50 pF, SN54HC541

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	2 V			171	ns
			4.5 V			34	
			6 V			29	
t_{en}	$\overline{OE}$	Y	2 V			224	ns
			4.5 V			45	
			6 V			38	
t_{dis}	$\overline{OE}$	Y	2 V			224	ns
			4.5 V			45	
			6 V			38	
t_t		Y	2 V			90	ns
			4.5 V			18	
			6 V			15	

6.10 Switching Characteristics, C_L = 50 pF, SN74HC541

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	2 V			144	ns
			4.5 V			29	
			6 V			25	
t_{en}	$\overline{OE}$	Y	2 V			188	ns
			4.5 V			38	
			6 V			32	
t_{dis}	$\overline{OE}$	Y	2 V			188	ns
			4.5 V			38	
			6 V			32	
t_t		Y	2 V			75	ns
			4.5 V			15	
			6 V			13	

6.11 Switching Characteristics, C_L = 150 pF, T_A = 25°C

over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	2 V		65	165	ns
			4.5 V		16	33	
			6 V		14	28	
t_{en}	$\overline{OE}$	Y	2 V		100	200	ns
			4.5 V		20	40	
			6 V		17	34	
t_t		Y	2 V		45	210	ns
			4.5 V		17	42	
			6 V		13	36	

6.12 Switching Characteristics, C_L = 150 pF, SN54HC541

over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	2 V			246	ns
			4.5 V			49	
			6 V			42	
t_{en}	$\overline{OE}$	Y	2 V			298	ns
			4.5 V			60	
			6 V			51	
t_t		Y	2 V			315	ns
			4.5 V			63	
			6 V			53	

6.13 Switching Characteristics, C_L = 150 pF, SN74HC541

over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	A	Y	2 V			206	ns
			4.5 V			41	
			6 V			35	
t_{en}	$\overline{OE}$	Y	2 V			250	ns
			4.5 V			50	
			6 V			43	
t_t		Y	2 V			265	ns
			4.5 V			53	
			6 V			45	

6.14 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	No load	35	pF

6.15 Typical Characteristics

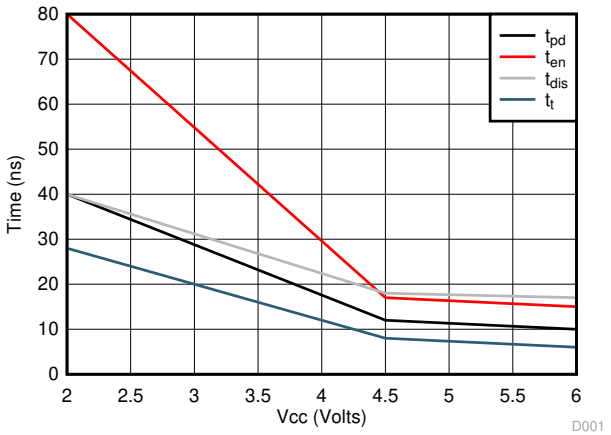


图 6-1. Typical Delay vs. V_{CC} for C_L = 50 pF

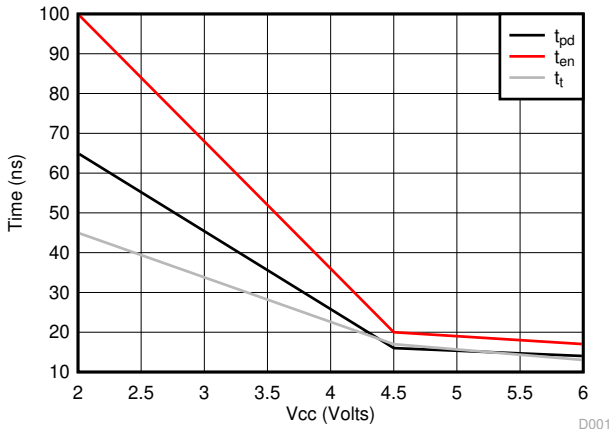
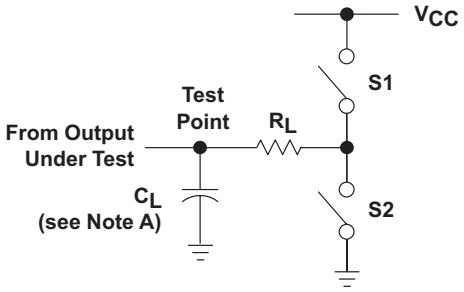


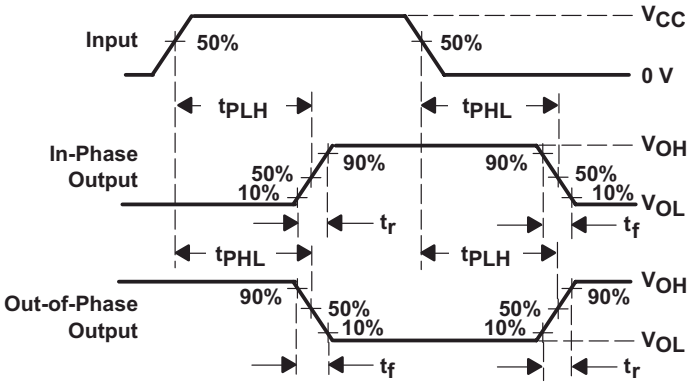
图 6-2. Typical Delay vs. V_{CC} for C_L = 150 pF

7 Parameter Measurement Information

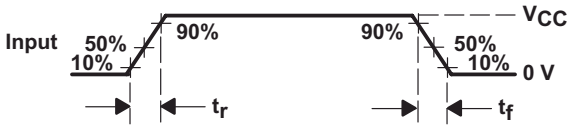


LOAD CIRCUIT

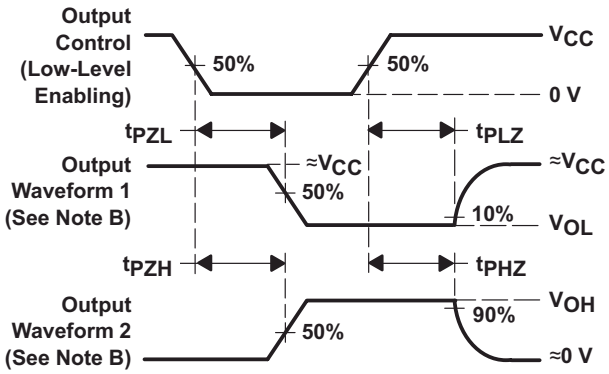
PARAMETER		RL	CL	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		—	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ⩽ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

图 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74HC541 device has 8 inputs and outputs where data from the A inputs go to the Y outputs. The output enables of the device control whether the information from the A inputs go to the Y outputs. These enable pins cause the device to go into high Z if either $\overline{OE1}$ or $\overline{OE2}$ are high. The $\overline{OE}$s should be tied to V_{CC} through a pull up resistor to ensure the high impedance state during power up or power down; the minimum value of the resistor is determined by the current sinking capability of the driver.

8.2 Functional Block Diagram

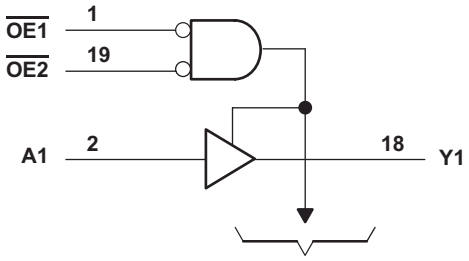


图 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

The SNx4HC541 has a wide operating voltage range of 2 V to 6 V. The device has multiple enable pins, and the device pinout enables simple board layout with outputs across from inputs.

8.4 Device Functional Modes

表 8-1 lists the functional modes of the SNx4HC541.

表 8-1. Function Table (Each Buffer/Driver)

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Hi-Z
X	H	X	Hi-Z

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

SN74HC541 is a wide range CMOS device that can be used over large voltage ranges. The device can be used anywhere from 2 to 6 Volts. The device can drive up to 6 mA of current at 5 Volts. This makes it perfect for driving bus lines directly or up to 15 LSTTL Loads. It can be used to drive anything from micro controllers and system logic devices to LEDs.

9.2 Typical Application

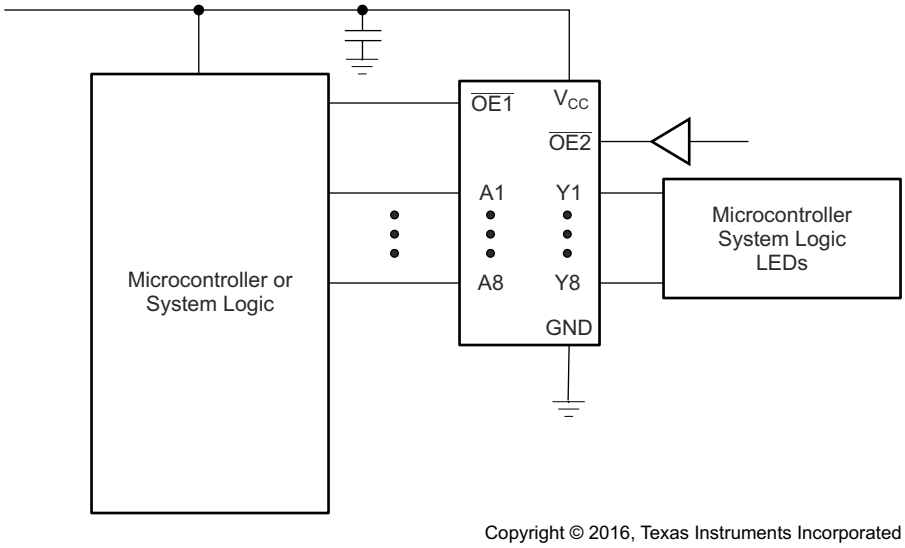


图 9-1. Typical Application Diagram

9.2.1 Design Requirements

This device uses CMOS technology and has a wide voltage range. Take care to avoid pulling too much current from the outputs as to not exceed 6 mA. Also, take care to not go over V_{CC} voltage to avoid damage to the device.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs: See ($\Delta t/\Delta V$) in the 节 6.3 table.
   - Specified high and low levels: See (VIH and VIL) in the 节 6.3 table.
   - Inputs should not be pulled above V_{CC}.
2. Recommended Output Conditions
   - Load currents should not exceed 6 mA for the part
   - Outputs should not be pulled above V_{CC}.

9.2.3 Application Curve

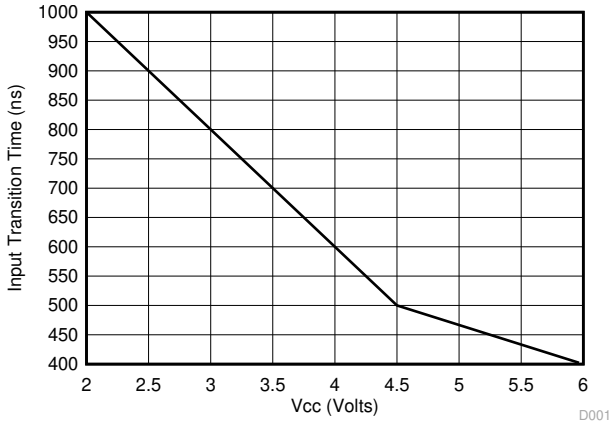


图 9-2. Input Transition Time vs. V_{CC}

10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the 节 6.3 table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1- μF is recommended; if there are multiple V_{CC} pins, then 0.01- μF or 0.022- μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1- μF and a 1- μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. The 节 6.3 section specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted. This does not disable the input section of the I/Os, so they cannot float when disabled.

11.2 Layout Example

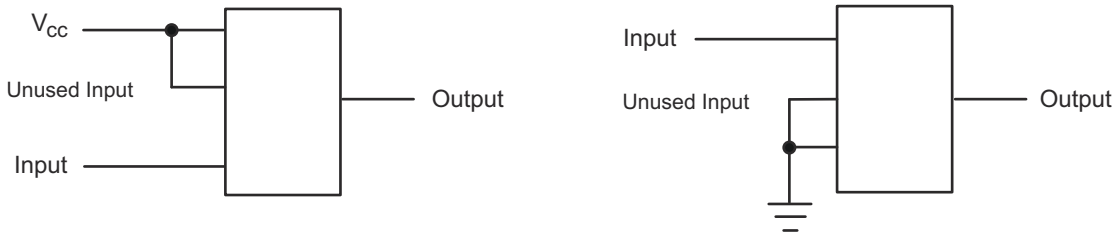


图 11-1. Layout Diagram

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HC541	Click here	Click here	Click here	Click here	Click here
SN74HC541	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/65711BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65711BRA	Samples
M38510/65711BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65711BRA	Samples
SN54HC541J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HC541J	Samples
SN74HC541DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC541	Samples
SN74HC541DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC541	Samples
SN74HC541DWE4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC541	Samples
SN74HC541DWG4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC541	Samples
SN74HC541DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC541	Samples
SN74HC541N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC541N	Samples
SN74HC541NE4	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC541N	Samples
SN74HC541NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC541	Samples
SN74HC541PW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC541	Samples
SN74HC541PWG4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC541	Samples
SN74HC541PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC541	Samples
SN74HC541PWT	ACTIVE	TSSOP	PW	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC541	Samples
SNJ54HC541FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54HC 541FK	Samples
SNJ54HC541J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54HC541J	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54HC541, SN74HC541 :

- Catalog : SN74HC541
- Military : SN54HC541

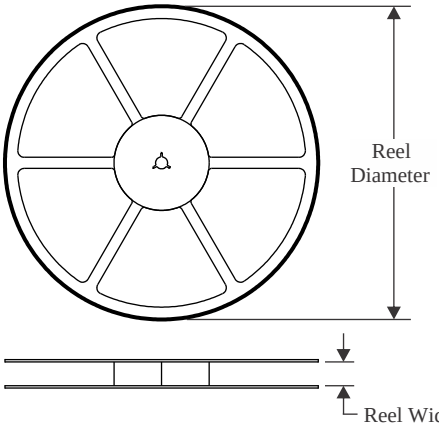
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

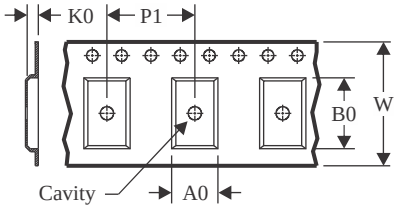
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

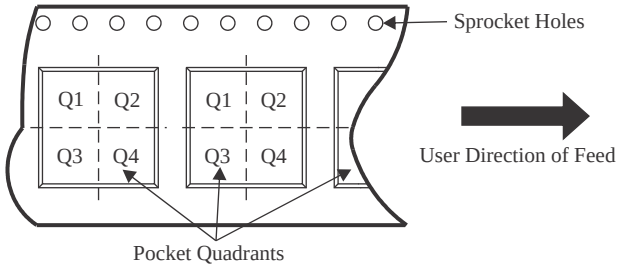


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

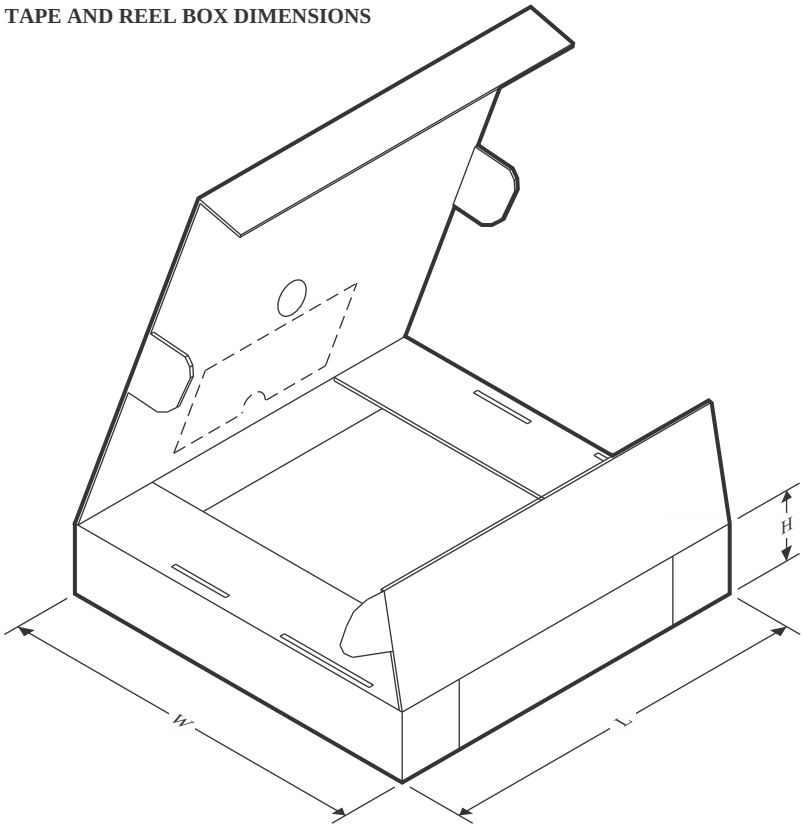
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC541DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HC541DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HC541DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74HC541NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HC541NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HC541PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HC541PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HC541PWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

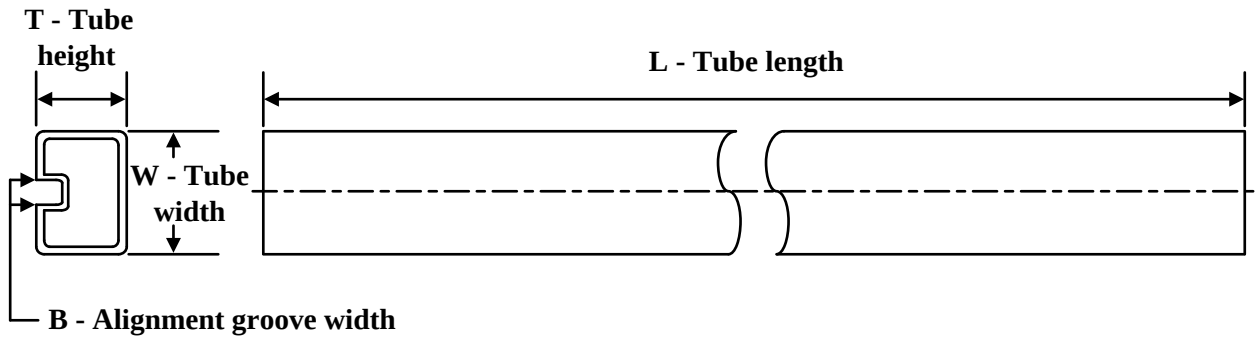
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC541DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74HC541DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74HC541DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HC541NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74HC541NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74HC541PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HC541PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HC541PWT	TSSOP	PW	20	250	356.0	356.0	35.0

TUBE



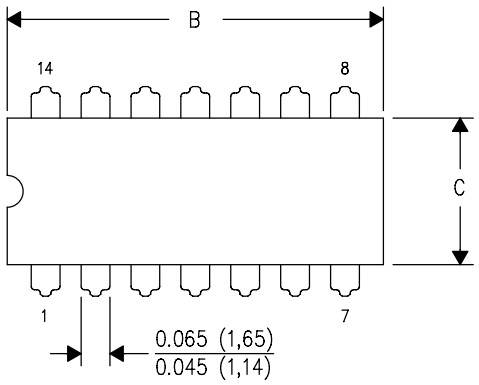
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74HC541DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74HC541DWE4	DW	SOIC	20	25	507	12.83	5080	6.6
SN74HC541DWG4	DW	SOIC	20	25	507	12.83	5080	6.6
SN74HC541N	N	PDIP	20	20	506	13.97	11230	4.32
SN74HC541NE4	N	PDIP	20	20	506	13.97	11230	4.32
SN74HC541PW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74HC541PWG4	PW	TSSOP	20	70	530	10.2	3600	3.5
SNJ54HC541FK	FK	LCCC	20	1	506.98	12.06	2030	NA

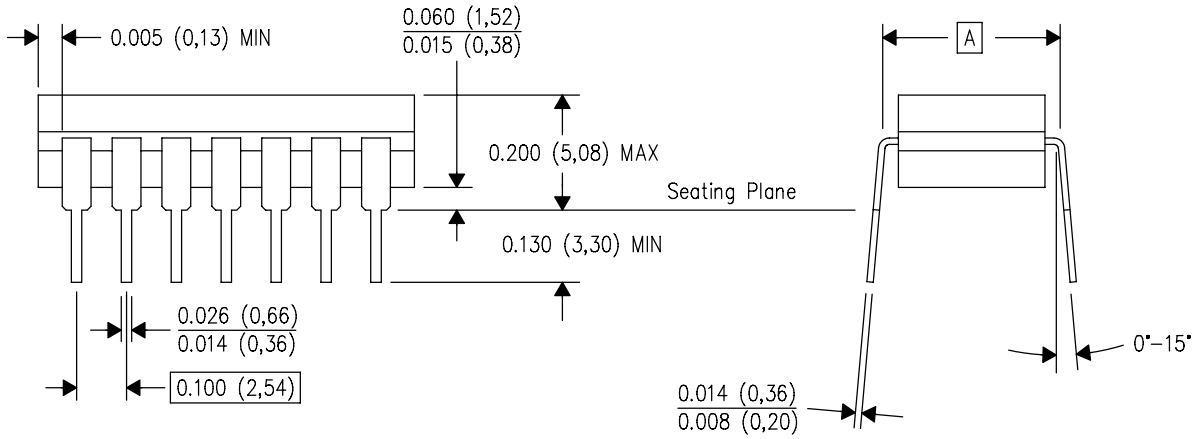
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



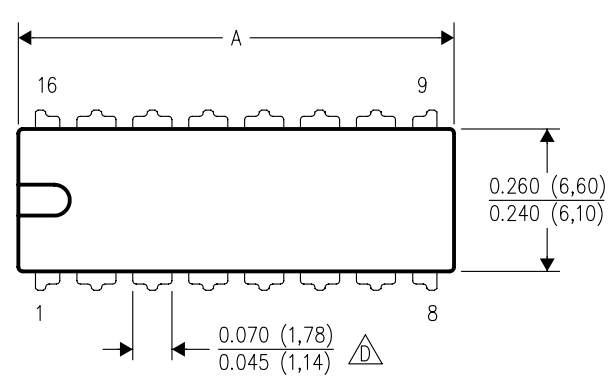
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

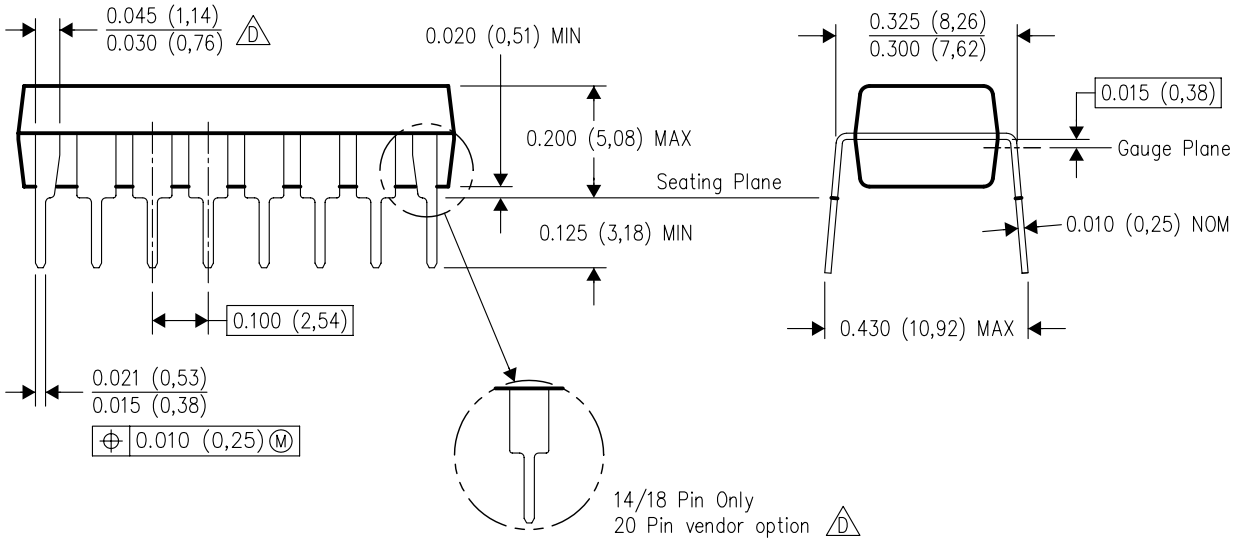
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

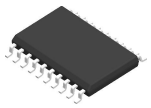


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

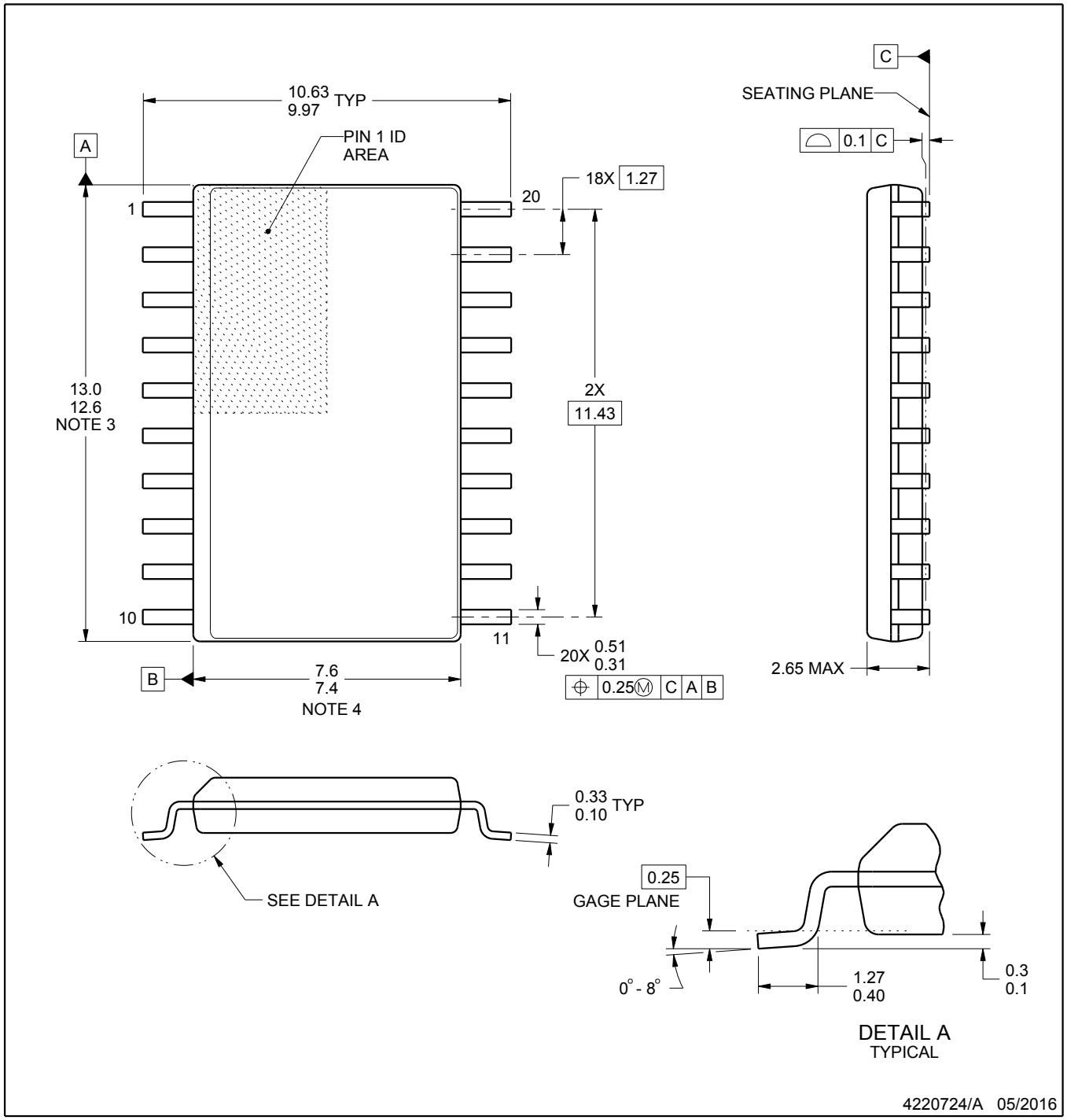


PACKAGE OUTLINE

DW0020A

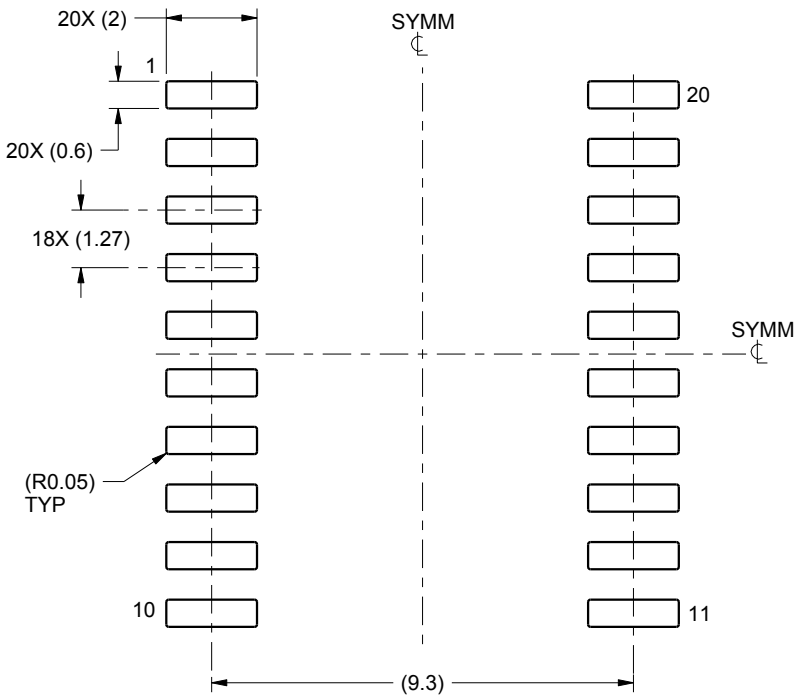
SOIC - 2.65 mm max height

SOIC

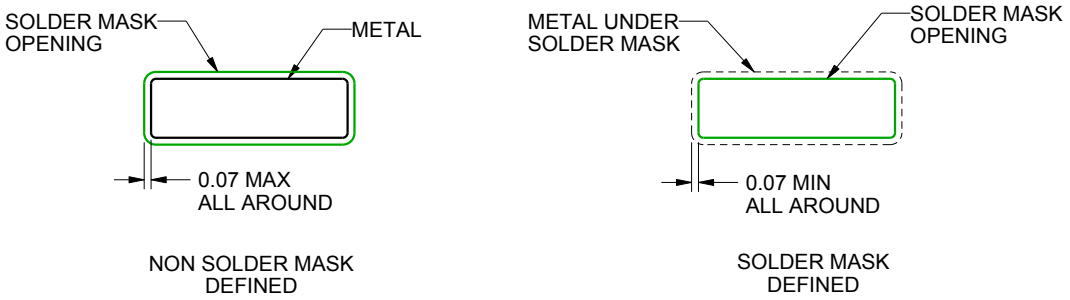


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

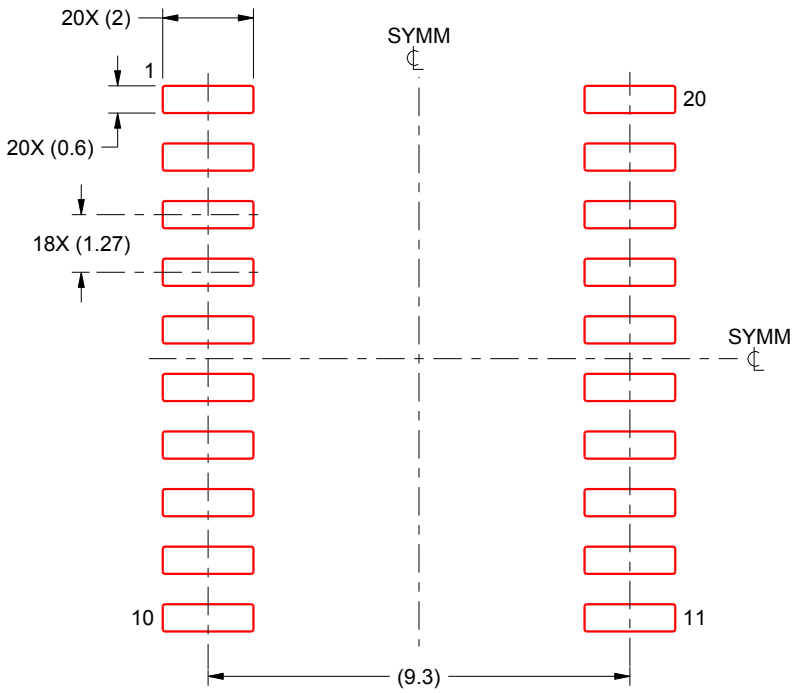


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

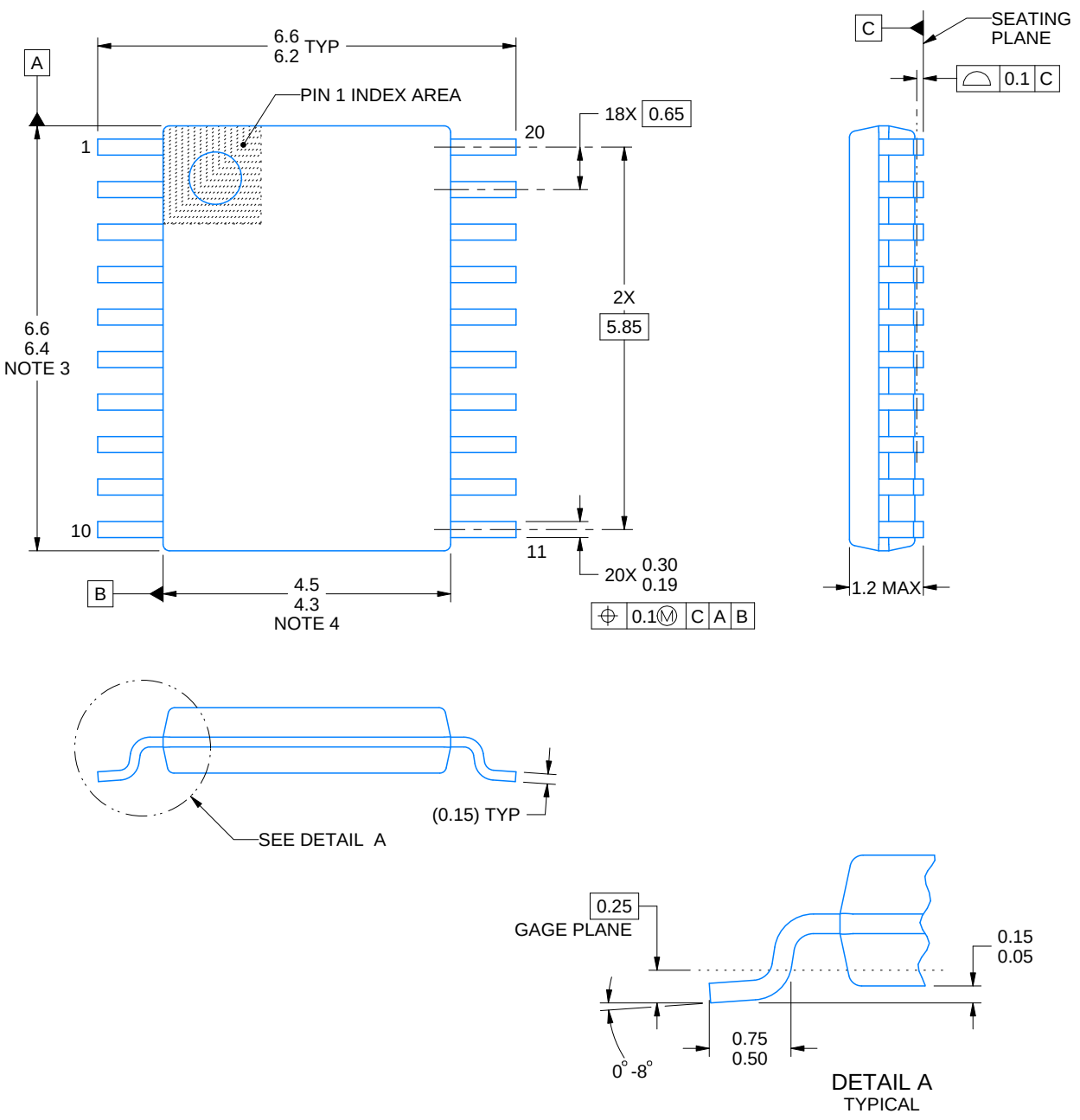
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0020A

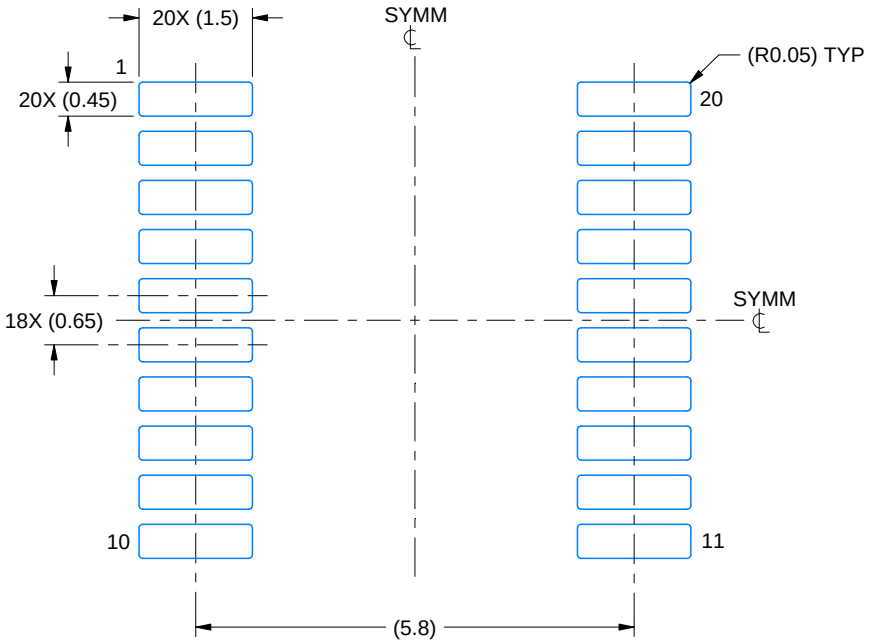
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



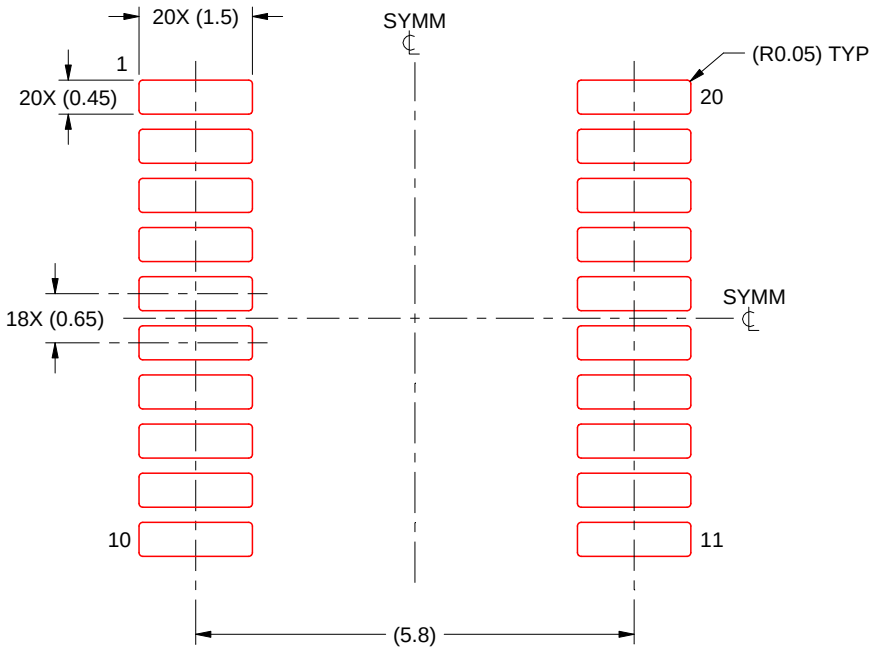
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



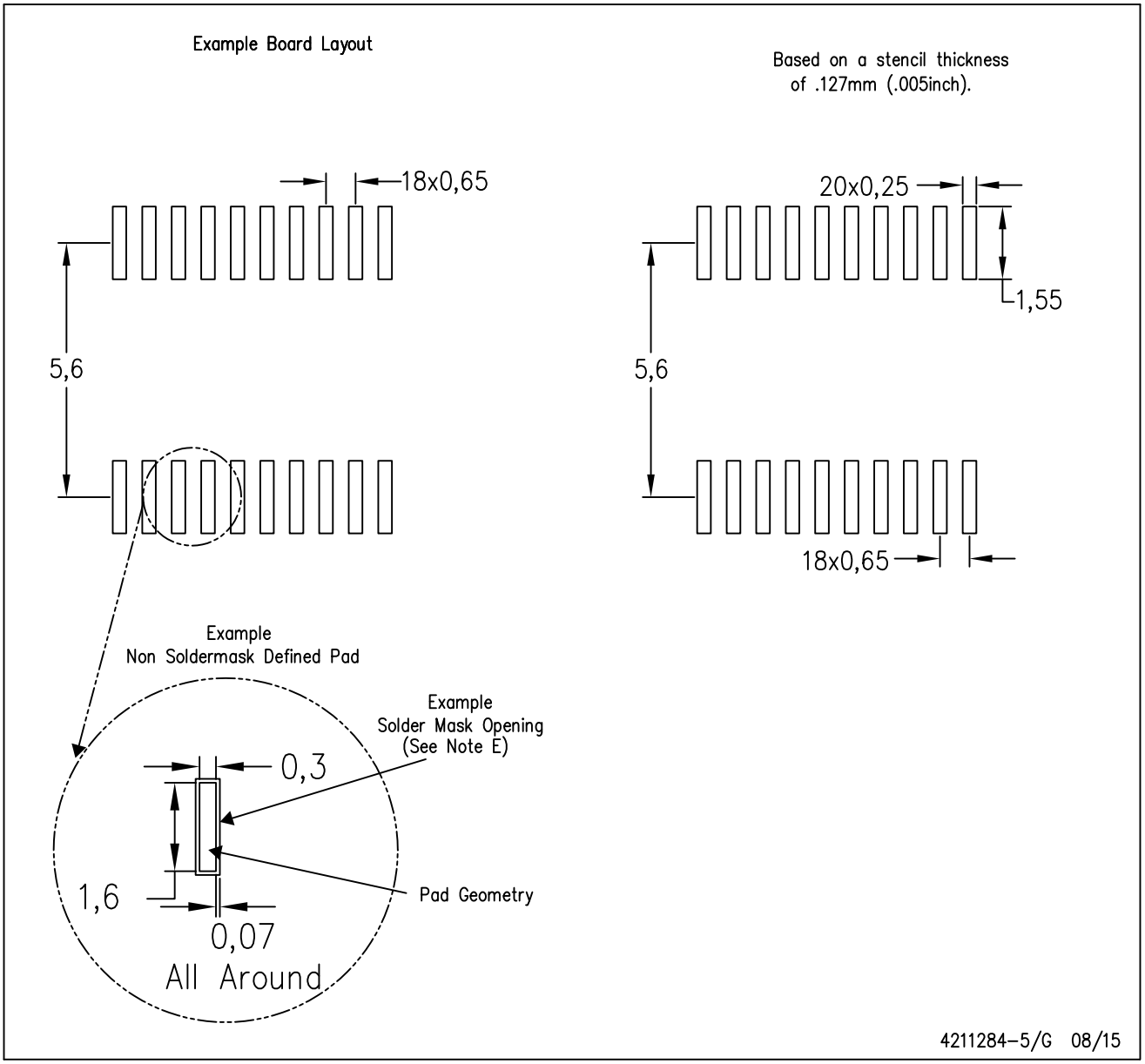
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

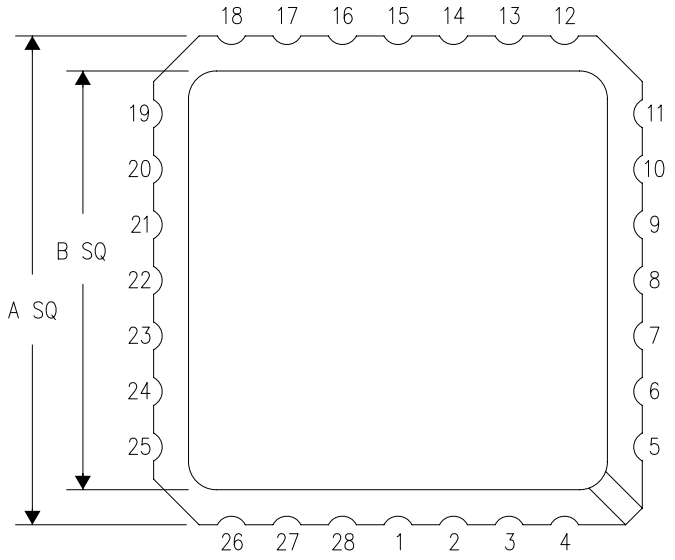
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



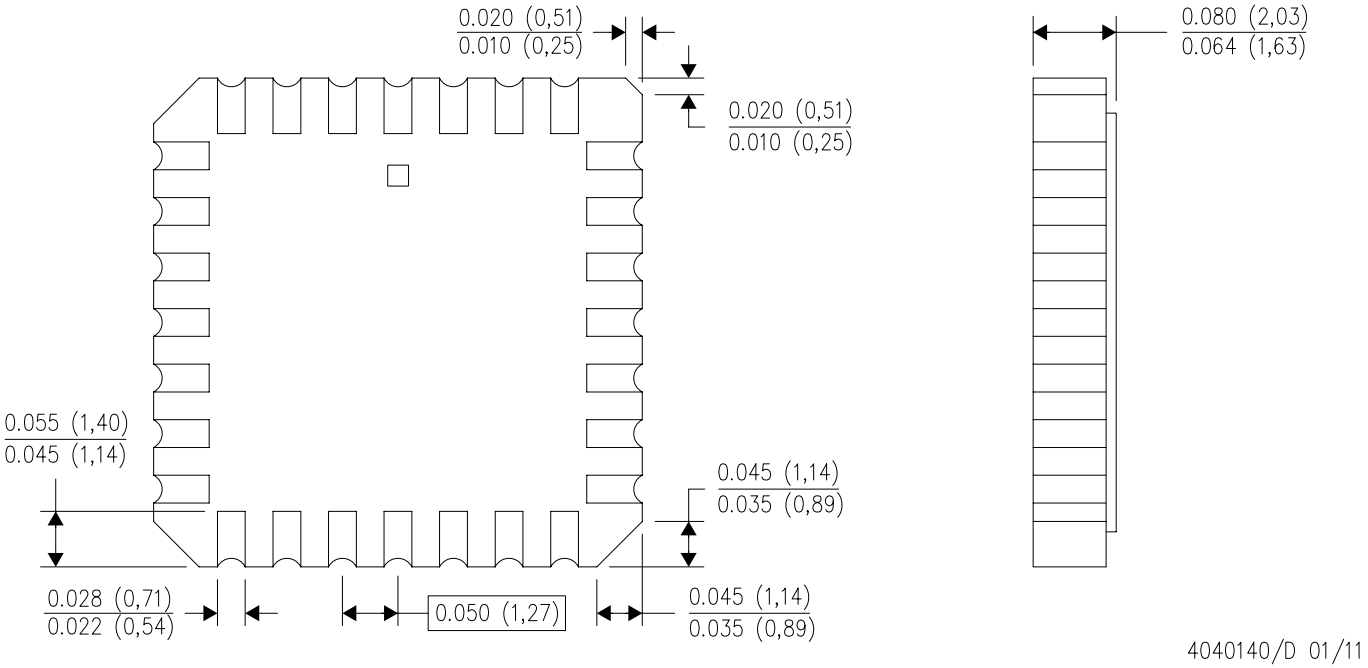
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

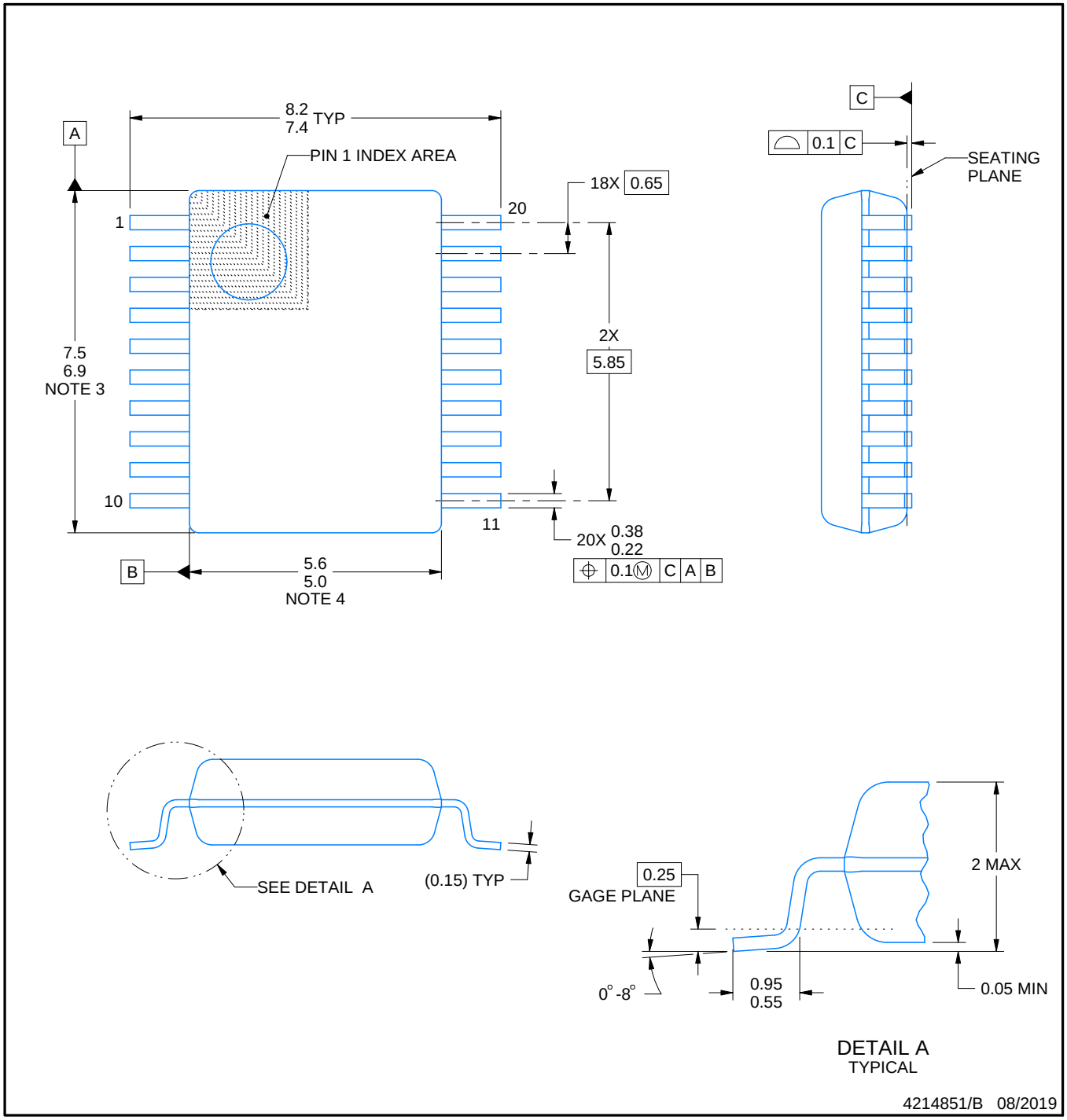
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

PACKAGE OUTLINE

DB0020A

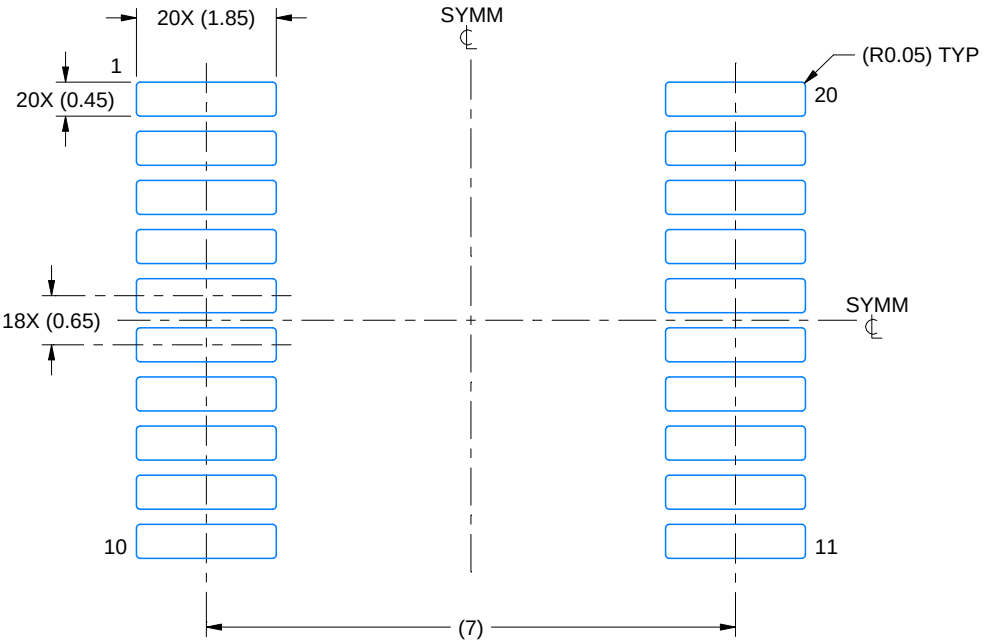
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

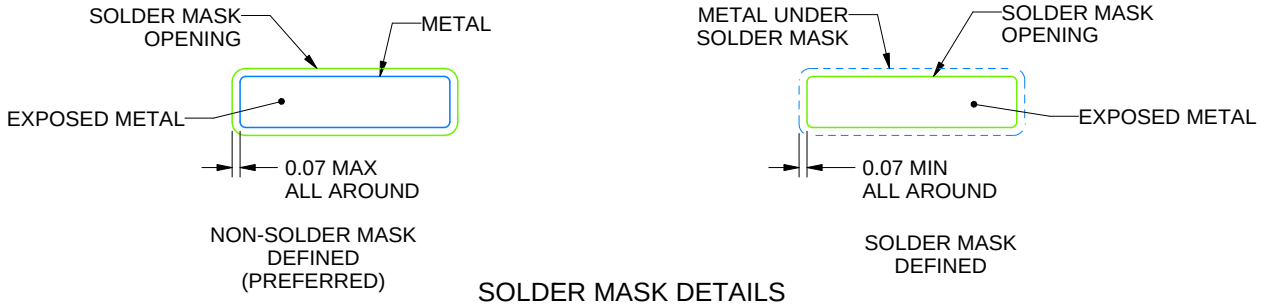


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

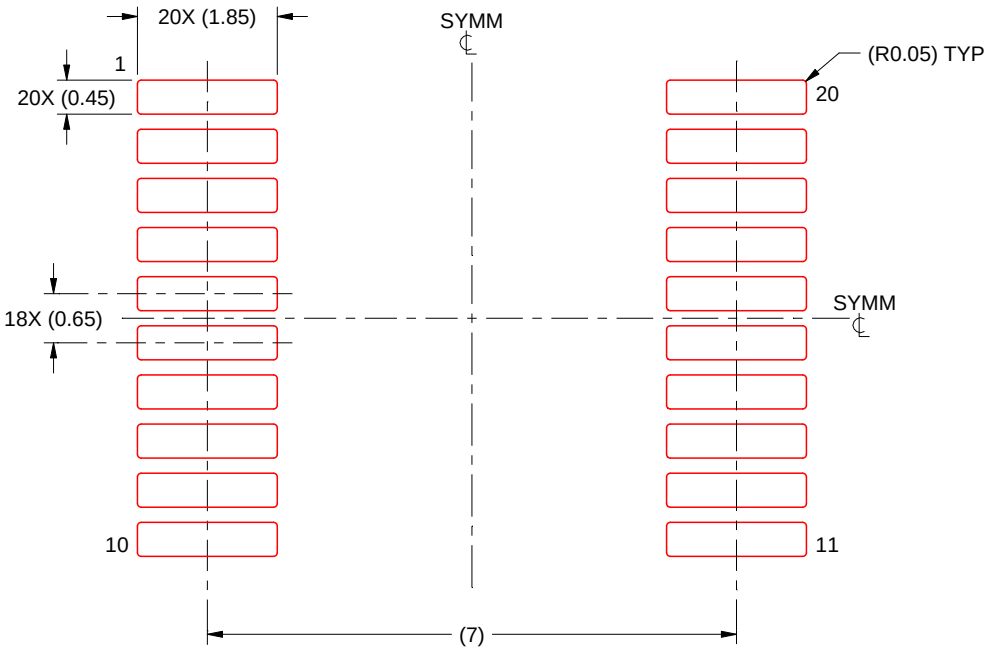
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

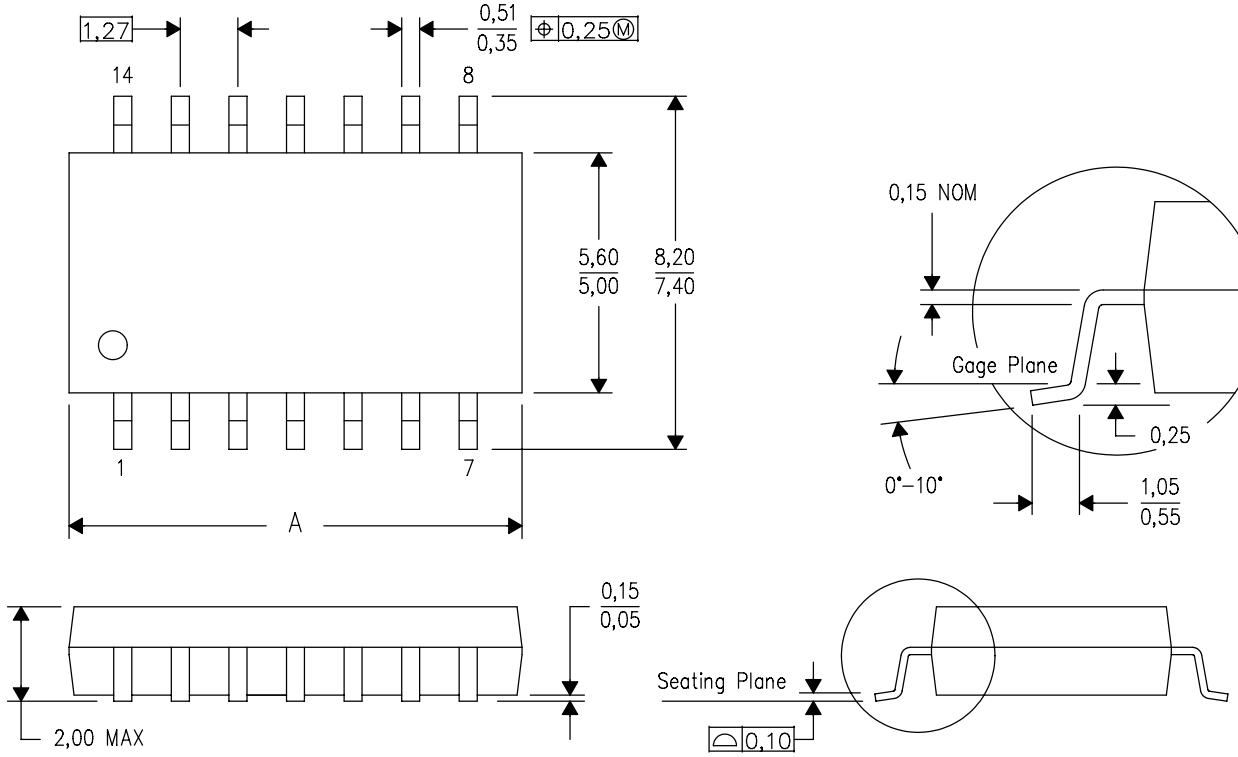
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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